IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

PROMOS TECHNOLOGIES, INC.,	)	
	)	
Plaintiff,	)	
	)	
v.	)	Civil Action No. 06-788 (JJF)
	)	
FREESCALE SEMICONDUCTOR, INC.,	)	
	)	
Defendant.	)	

PLAINTIFF PROMOS TECHNOLOGIES, INC.'S
ANSWERING CLAIM CONSTRUCTION BRIEF

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INTRODUCTION

A consistent theme and flaw in the Opening Brief filed by Freescale Semiconductor, Inc. ("Freescale") is that it seeks to have the Court limit the claims of the patents-in-suit in ways that are both contrary to the claim language and unsupported by anything else in the intrinsic record. That, of course, is contrary to governing law. Lucent Techs., Inc. v. Extreme Networks, Inc., 367 F. Supp. 2d 649, 653 (D. Del. 2005) ("The starting point for a claim construction analysis is the claims themselves," and "there is a strong presumption in favor of the ordinary meaning of claim language") (and Federal Circuit precedent cited therein).

With respect to the Chan '709 and '241 patents, Freescale repeatedly makes bold promises on which its brief never delivers. In particular, Freescale's brief flatly asserts every few pages that "the prosecution history, specification, and claims make clear that the '709 and '241 claims are directed to a cache chip that is external to the CPU." See Freescale's Opening Brief ("FSI Br.") at 21. But it does not quote a single statement from the prosecution history or specification that backs up that assertion or others like it. At the same time, the language of the '709 and '241 patent claims actually contradicts Freescale's purported "external" or "separate-chip" limitation, which is why Freescale has been forced to scour the prosecution history and specification in a futile effort to find a basis for that limitation before even turning to the claims themselves. In short, Freescale goes beyond a mere attempt to import limitations from the specification into the claims (see FSI Br. at 32-33); it seeks to import limitations that are found nowhere in the specification or prosecution history. That approach must be rejected.

With respect to the Fortin '267 patent, Freescale as much as acknowledges that its claim construction positions are driven by its desire to develop non-infringement positions. Early in its brief, Freescale argues that its "accused Hip7 and HiP8 processes" use chemical vapor deposition ("CVD") "instead of" physical vapor deposition ("PVD"). FSI Br. at 6. Not only is that argument premature by several months, and not only does it overlook that an accused process may use CVD *as well as* PVD, but it also reveals the purpose behind Freescale's proposed constructions of Fortin patent terms. Freescale proposes a construction of "PVD", for example,

that includes an addendum that "Chemical vapor deposition is not physical vapor deposition or a type of physical vapor deposition." That addendum, like a similar one tacked on to the end of Freescale's proposed construction of "CVD", can serve no purpose other than to build support for a non-infringement argument regarding the accused Hip7 and HiP8 processes. Such a purpose is plainly inappropriate in the Markman process. Young Dental Mfg. Co. v. Q3 Special Prods., Inc., 112 F.3d 1137, 1141 (Fed. Cir. 1997). Accordingly, the Court should reject Freescale's proposed construction of the terms of the Fortin patent in favor of the straightforward constructions proposed by ProMOS Technologies, Inc. ("ProMOS").

I. FREESCALE'S ERRONEOUS CONSTRUCTION OF THE CHAN PATENT CLAIM TERMS.

The arguments presented by Freescale on the Chan '709 and '241 patents are closely analogous – indeed, remarkably so – to arguments that this Court *rejected* in its 2005 Markman ruling in Lucent Techs. v. Extreme Networks, supra. In Lucent, the defendants argued that two patents addressing problems of congestion in "packet switching telecommunications networks" (the '810 and '811 patents) should be limited to "networks comprised of virtual circuits," even though the claims did not include a "virtual circuit" limitation. The Lucent defendants reasoned that such a limitation was appropriate because the specification and prosecution history described "the invention" of the '810 and '811 patents as involving networks comprised of virtual circuits, and because every embodiment in the patents utilized virtual circuits. Id. at 654-55. This Court nonetheless soundly rejected those arguments, based on governing Federal Circuit authority, because Lucent had "not made a clear disavowal of embodiments lacking virtual circuits." Id.[1]

In advancing its arguments, Freescale relies on an overly broad reading of the same Federal Circuit holdings that this Court properly interpreted and applied in a much more limited

[1] The defendants in Lucent also argued that the '810 patent should be limited to networks that utilize "packet monitoring and marking" at an "access node", because that is how "the invention" purportedly was described in the '810 specification. Again, this Court rejected that limitation because the defendants merely cited to "language that can reasonably be understood as constituting general description of the invention," without "clearly defin[ing] the term 'node' as meaning 'access node,'" and they "point[ed] to no clear disavowal of claim scope in either the written description or prosecution history." Id.

manner in Lucent.[2] In fact, the arguments advanced by Freescale for an implied limitation of the Chan patent claims to "external" or "separate-chip" cache memories are far weaker than the implied limitation arguments that this Court rejected in Lucent. At most, Freescale has been able to point to places in the prosecution history and specification in which the patentee showed how his invention could be implemented using a separate cache memory chip, or how such an embodiment could be implemented "in accordance with the invention." FSI Br. 28-31. Freescale never identifies any "broad, unequivocal statement" in the intrinsic record that describes the invention itself as requiring a separate cache memory chip, Lucent, 367 F. Supp. 2d at 654, and it utterly fails to deliver on its promise to show that "The Chan Specification Disclaimed An Internal Cache." Id. at 31-32. If such a clear statement of the scope of the invention or such a disclaimer existed, one reasonably would expect it to be quoted in Freescale's brief, most likely in bold print. But Freescale has provided no such quote.

Instead, Freescale has relied on weak and strained inferences of the type that this Court rejected in Lucent. Freescale also has ignored the fact that the Chan specification actually *disclaims* the very *disclaimer* that Freescale's Brief promises to produce but never actually delivers. In the "Summary of Invention" portion of the specification, which is where one might reasonably expect to find any statements limiting the scope of the invention as a whole, Lucent, 367 F. Supp. 2d at 654, the Chan patents make clear that no such scope limitations are intended or should be inferred: "As will be appreciated by one skilled in the art, the invention is applicable to cache memory systems in general, and is not limited to the specific embodiment disclosed." See '709 patent 4:22-26. Freescale efforts to read an "external" or "separate-chip" limitation into the Chan patents infects virtually every one of its proposed constructions. For that

[2] Compare FSI Br. at 33, 37 (arguing that, under Microsoft Corp. v. Multi-Tech Sys., Inc., 357 F.3d 1340 (Fed. Cir. 2004), because figures in the Chan patents are described as being "in accordance with the invention," "the invention" must be limited to the embodiments in those figures); with Lucent, 357 F. Supp. 2d at 654 (recognizing that in Microsoft the Federal Circuit addressed a specification that "repeatedly and consistently describe[d] the claimed inventions" as being subject to the asserted limitation, including in the Summary of Invention portion, which clearly was "not limited to describing a preferred embodiment, but more broadly describe[d] the overall invention").

reason, as well as others discussed below, the Court should reject all of Freescale's proposed constructions and adopt those proposed by ProMOS for the terms of the Chan patents.

A. Freescale's Argument That The Chan Patents Are Limited To An "External Cache Chip" Is Contrary To The Claim Language And Unsupported By The Specification Or The Prosecution History.

Freescale argues at length that all the claims of the Chan patents are limited to "external" cache memory, which it in turn defines to mean a "cache memory chip" that is separate from the chips that contain the CPU and system memory. See FSI Br. at 19-33. That argument is inconsistent with the ordinary meaning of "cache memory," and it further runs afoul of the principle that "modifiers will not be added to broad terms standing alone." Johnson Worldwide Assocs., Inc. v. Zebco Corp., 175 F.3d 985, 989 (Fed. Cir. 1999); accord, e.g., Virginia Panel Corp. v. MAC Panel Co., 133 F.3d 860, 865-66 (Fed. Cir. 1997). In advancing this argument, Freescale seeks to turn on its head the proper approach to claim construction, first directing its attention to the prosecution history of the Chan patents, then to the specification, and finally to the claim language itself. Lucent, 367 F. Supp. 2d at 653 ("The starting point for a claim construction analysis is the claims themselves"); accord, e.g., Phillips v. AWH Corp., 415 F.3d 1303 (Fed. Cir. 2005) (claim language is of "primary" importance). Because none of those sources support Freescale's argument, it does not matter in what order they are addressed; there is no basis for reading into the Chan patents an "external" or "separate chip" limitation.

1. The Prosecution History Does Not Support Freescale's Argument.

Freescale first argues that the prosecution history supports its assertion that the claimed cache memory must be external to the processor. FSI Br. at 25-29. However, Freescale has not shown that the patentee ever disclaimed internal cache memories or argued patentability over prior art on the basis of an external/internal or separate-chip distinction, nor has Freescale provided any basis for asserting that the examiner's allowance of the claims without any "external chip" limitation was in error. Id. That failure is telling. Prosecution history may not be used to infer the narrowing of a claim unless the applicant makes a disclaimer with "clarity

and deliberateness." N. Telecom Ltd. v. Samsung Elecs. Co., Ltd., 215 F.3d 1281, 1294-5 (Fed. Cir. 2000) (where remarks made to overcome prior art do not "specifically state [the] exclusion" of subject matter, they are "far too slender a reed to support the judicial narrowing of a clear claim term"); accord, e.g., Rexnord Corp. v. Laitram Corp., 274 F.3d 1336, 1347 (Fed. Cir. 2001) (refusing to limit the ordinary meaning of a claim based on an "inconclusive" disclaimer); Lucent, 367 F. Supp. 2d at 656 (there is no disclaimer where there is "no clear disavowal of claim scope" in the prosecution history).

Freescale predicates its muddled prosecution history disclaimer argument on the fact that (i) the applicant attached datasheets to his *original, abandoned* application for products which happened to be "external" cache products, although he did not highlight them as being such, FSI Br. at 26;[3] and (ii) when the examiner rejected an earlier set of claims based on indefiniteness grounds and on the failure to describe the invention in patentably distinct terms, the applicant responded by citing to language in the specification similar to language contained in the datasheets. FSI Br. at 29. Notably, Freescale has not argued that the applicant ever amended the claims to reference the "external" limitation that it now seeks to impose on the plain meaning of "cache memory," nor has Freescale argued that either the examiner or the patentee even referenced or addressed the purported "internal/external" distinction. Rather, Freescale asserts that the mere attachment of Mosel datasheets to the original abandoned application reflects some unspoken intention on the part of the applicant to limit his invention to the specific products described in the data sheets, which just happened to be "external" caches. FSI Br. at 28. Such vague assertions, based on speculation and a strained interpretation of the prosecution history, cannot substantiate a disclaimer of internal caches by the applicant, let alone one made with "clarity and deliberateness." N. Telecom Ltd., 215 F.3d at 1294-5; Lucent, 367 F. Supp. 2d at 654-56.

[3] Freescale errs as a matter of law in relying on the original application, which Chan abandoned in favor of a more detailed specification following an indefiniteness (§ 112, ¶ 2) rejection. See Waldemar Link, GmbH & Co. v. Osteonics Corp., 32 F.3d 556, 559-560 (Fed. Cir. 1994) (absent a section 112, ¶ 1 rejection, there is no estoppel that arises from the filing of a continuation-in-part application).

Indeed, Freescale's implicit suggestion that either the patentee or the examiner viewed "internal" cache memories as unpatentable over the prior art makes no sense, both because the issue was not raised anywhere in the prosecution history and because there was nothing novel about "external" cache memories. The specification explicitly discloses that both "internal" and "external" cache memories were known in the prior art – and external cache memories came first. '709 patent, 2:66-3:1. Even assuming for the sake of argument, however, that the examiner had viewed the "external" nature of the cache memory to be critical to patentability, he would have said so and required a specific amendment of the claims to reflect that requirement. Rexnord Corp., 274 F.3d at 1347 ("if the examiner wanted to hinge patentability upon the 'link module portion' being structurally separate from the 'cantilevered portion,' he would have said so, and required a specific amendment to reflect the separate structures."). For the foregoing reasons, there simply can be no suggestion that the prosecution history supports Freescale's assertion that the cache memory must be "external" to the processor.

2. The Specification Does Not Support Freescale's Argument.

The specification similarly provides no support for Freescale's argument that the claimed cache memory must be "external" to the CPU or on a separate chip. In fact, the specification does not even address the internal/external distinction that permeates Freescale's brief, other than to note in its discussion of the prior art that cache memory may be *either* internal *or* external to the CPU. '709 patent, 2:66-3:1. The only support that Freescale has proffered for its assertion that the claimed cache memory must be limited to an "external chip" is to cite a specific embodiment described in the specification. FSI Br. at 29-31. But the Federal Circuit has cautioned against using the specification and embodiments described therein to alter the plain meaning of claim terms. See JVW Enters., Inc. v. Interact Accessories, Inc., 424 F.3d 1324, 1335 (Fed. Cir. 2005) ("We do not import limitations into claims from examples or embodiments appearing only in a patent's written description, . . . unless the specification makes clear that 'the patentee … intends for the claims and the embodiments in the specification to be strictly

coextensive.'"); Callicrate v. Wadsworth Man., Inc., 427 F.3d 1361, 1368 (Fed. Cir. 2005) (same); Liebel Flarsheim Co. v. Medrad, Inc., 358 F.3d 898, 908 (Fed. Cir. 2004) (same); Lucent, 367 F. Supp. 2d at 655 (finding no "clear disavowal of embodiments lacking virtual circuits" even though "every embodiment of the invention disclosed in the specification of these patents utilizes virtual circuits"); see also Cordis Corp. v. Medtronic Ave., Inc., 339 F.3d 1352, 1365 (Fed. Cir. 2003) (Under 35 U.S.C. § 112, ¶ 1, a specification may "contain a written description of a broadly claimed invention without describing all species that the claim encompasses.").

Freescale attempts to sidestep this fatal flaw in its argument by representing to the Court that the specification "consistently describes a cache memory chip that is external to the CPU as '*the invention*.'" FSI Br. at 29. Freescale apparently did not expect the Court to read the Chan specification itself, because the specification passages cited by Freescale merely describe embodiments as being "in accordance with the invention"; they do not purport to limit "the invention" itself. See '709 patent, 7:7-15 (describing Figs. 8A-8C as "a diagram of the burst RAM cache memory chip *in accordance with* the invention"); 6:49-54 (describing Fig. 6 as "a burst RAM cache memory *in accordance with* the present invention"); 72:59-61 (describing Fig. 58 as the "burst RAM cache memory chip *in accordance with* the invention"). The patentee's use of the phrase "*in accordance with* the present invention" makes clear that he was merely providing examples of embodiments that practice the claimed invention, as opposed to limiting the invention's scope. The cases cited by Freescale thus are readily distinguishable.

Freescale further argues that the patentee "disclaimed" an internal cache by "illustrating the drawback" of a referenced internal cache of an Intel 486 processor. FSI Br. at 31. To narrow the scope of claims, however, the specification must reflect a "*clear disclaimer* of particular subject matter." Liebel Flarsheim Co., 358 F.3d at 909 (emphasis added); Lucent, 367 F. Supp. 2d at 654. The Chan specification does nothing of the sort; in fact, the specification makes clear that "the invention is applicable to cache memory systems in general." '709 patent, 4:22-26. The passage relied on by Freescale merely notes that the Intel 486 processor utilizes four data cycles. '709 patent, 3:16-33. It does not indicate that this functionality relates to the Intel 486

processor's internal cache, nor does it identify any problems associated with data cycles that may be avoided by using an external cache. Moreover, the specification does not purport to distinguish or claim improvement over the prior art based on the use of an external cache.[4] For these reasons, this case is distinguishable from the pre-Phillips cases cited by Freescale, both of which involved specifications that highlighted the asserted limitation as the novel improvement over prior art. SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys., 242 F.3d 1337, 1343-44 (Fed. Cir. 2001) (specification distinguished prior art based on use of specific structures which it unequivocally stated "all embodiments of the present invention" must contain); Alloc, Inc. v. ITC, 342 F.3d 1361, 1344 (Fed. Cir. 2003) (specification identified "play" in floor panels as key improvement and described invention as "directed toward flooring products including play").[5]

The Federal Circuit's ruling in SunRace Roots Enter. Co. LTD v. SRAM Corp., 336 F.3d 1298 (Fed. Cir. 2003), is also instructive. In that case, the dispute centered on whether the claims should be read to include a cam as part of the recited shift actuator. The Federal Circuit held that they should not, noting: "[n]othing in the written description indicates that the invention is *exclusively directed* toward cams or suggests that systems not employing cams are *outside the scope of the invention.* Thus, while it is clear that the patentee was primarily focused on an embodiment of the invention using a cam, nothing in the patent limits the claims to that embodiment." Id. at 1305 (emphasis added). So too here. The fact that embodiments in the '709 patent specification are depicted with external caches does not establish a "clear disclaimer" of internal caches from the scope of the claims. Liebel Flarsheim Co., 358 F.3d at 909.[6]

[4] Indeed, it would have made little sense for the patentee to have made this assertion, because external caches were known in the prior art and therefore were not novel. '709 patent, 2:64-3:1.

[5] Freescale also cites to a case involving amendments and arguments made before the PTO disclaiming subject matter to overcome prior art during prosecution of a patent. See FSI Br. at 25, 31, citing Chimie v. PPG Indus. Inc., 402 F.3d 1371, 1384 (Fed. Cir. 2005). That is not the situation here.

[6] Accord Lucent, 367 F. Supp. 2d at 654-66 (rejecting "virtual circuit" and "access node" limitations as not mandated by the specification); 664 (refusing to import limitation from Summary of Invention into claim term "integrated voice and data multiplexer"); 664 (construing "guaranteeing predetermined individual minimum bandwidths" based on general meaning, because description of invention in specification did not represent "a clear disavowal of claim scope"); 664-65 (rejecting proposed construction of "voice traffic" because Court does not find that specification's "description of the way the

3. The Claims of the Chan Patents Do Not Support Freescale's Argument.

Finally, and most importantly, Freescale has not suggested – nor could it suggest – that the claim language itself supports its argument that the claimed invention requires an "external cache chip." FSI Br. at 25-33. This failure is telling, because it is the *claims* of a patent that define the invention to which the patentee is entitled the right to exclude. Phillips v. AWH Corp., 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc). It is fundamental that "in construing claims, the analytical focus must begin and remain centered on the language of the claims themselves, for it is that language that the patentee chose to use to 'particularly point [...] out and distinctly claim [...] the subject matter which the patentee regards as his invention.' " Interactive Gift Express, Inc. v. Compuserve, Inc., 256 F.3d 1323, 1331 (Fed. Cir. 2001) (quoting 35 U.S.C. § 112). The claim language itself is "of primary importance, in the effort to ascertain precisely what it is that is patented." Phillips, 415 F.3d at 1312; see also Inverness Med. Switzerland GmbH v. Princeton Biomeditech Corp., 309 F.3d 1365, 1369 (Fed. Cir. 2002).

Courts indulge a " 'heavy presumption' that a claim term carries its ordinary and customary meaning." Teleflex, Inc. v. Ficosa N. Am. Group, 299 F.3d 1313, 1325 (Fed. Cir. 2002) (quotation omitted). As a matter of ordinary usage, the term "cache memory" as used in the claims encompasses both internal and external caches in the same way that the term "garage" encompasses both internal and external garages and the term "hard drive" encompasses both internal and external hard drives. Lest there be any remaining doubt about the meaning of "cache memory," the specification assuages it by expressly stating that to one skilled in the art, "[c]ache memory may be internal to the microprocessor, as in the model 80486 microprocessor of the Intel Corporation, or external." '709 patent, 2:66-3:1. For the foregoing reasons,

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voice packets are organized amounts to a definition of 'voice traffic' representing a clear disavowal of claim scope"); 665 (refusing to find "clear disavowal of claim scope" regarding claim term "data traffic"); 666 (construing "integrated first and second type of traffic multiplexer" in accordance with plain language of claim because general description in the specification "does not clearly define the term" so as to constitute "a clear disavowal of claim scope"); 667 (refusing to limit construction of "protocol for a data network" where the specification "has not made a clear disavowal of protocols used in networks other than Metropolitan Area Networks (MANs)," and "all the Defendants can point to in the specification is the absence of any embodiment that lacks an MAN").

Freescale's argument that the cache memory of the claimed invention must be on a separate chip from the processor must be rejected. As a result, the vast majority of Freescale's proposed constructions for individual terms fall of their own weight.

B. Freescale's Proposed Constructions of Individual Claim Terms That Should Be Construed By The Court Are Unsustainable.

1. "cache memory," Chan 241, claims 1, 15, and 16:

ProMOS Construction	Freescale Construction
Small block of high speed memory associated with a computer processor/microprocessor (CPU)	a memory chip that is external to the CPU chip

As noted in Section I.A above, the proposed "external" and "chip" limitations in Freescale's proposed construction of "cache memory" are not found anywhere in the claims. Moreover, they are in direct conflict with both the ordinary meaning of "cache memory" as well as the use of that term in the specification, which expressly states that to one skilled in the art a "cache memory" can be *either* external *or* internal to the microprocessor. '709 patent, 2:66-3:1.

As a result, Freescale is forced to premise its argument on the faulty assertion that the patentee "distinguished his invention from the prior art internal cache systems" in the specification and "relied on these differences to obtain the patents-in-suit from the Patent Office." FSI Br. at 36.[7] But as noted above, *nowhere* in the specification or prosecution history did the patentee express any intention to limit his invention to external cache memory rather than internal cache memory, or to cache memory on a different chip than the microprocessor. Indeed, Freescale has failed to identify any support at all from the prosecution history for its construction of the term "cache memory," FSI Br. at 35-36, and although Freescale misleadingly suggests that the patentee "distinguished his invention from the internal cache" by referencing a "cache memory chip" when describing his invention, FSI Br. at 36, the portions of the specification cited by Freescale do not distinguish the invention from the prior art or otherwise describe features as necessary for patentability. See '709 patent, 4:62-64; 6:58-60; 7:12-13, 10:38-50;

[7] For reasons that are not clear and not explained, Freescale seeks to support its argument on this point by citing a case involving "explicit arguments made during prosecution to overcome prior art." See FSI Br. at 36 (citing Spectrum Int'l, Inc. v. Sterilite Corp., 164 F.3d 1372, 1378-9 (Fed. Cir. 1998)).

72:60-61. Nor did the patentee ever state, as suggested by Freescale, that his "invention" was directed to cache memory on a separate chip from the CPU. FSI Br. at 36-37, citing '709 patent, 6:58-60; 7:12-13, 10:38-50; 72:60-61. Rather, the cited portions of the specification merely describe examples of how the invention might be implemented in particular embodiments "in accordance with" the invention. It is well settled that Freescale cannot read a limitation into the claims simply because certain embodiments in the specification depict the cache memory and CPU on different chips. Anchor Wall Sys., Inc. v. Rockwood Retaining Walls, 340 F.3d 1298, 1306-07 (Fed. Cir. 2003) ("the mere fact that the patent drawings depict a particular embodiment of the patent does not operate to limit the claims to that specific configuration"); TI Group Auto. Sys. v. VDO N. Amer., 375 F.3d 1126, 1138 (Fed. Cir. 2004) (same). In contrast, Chan expressly stated in the specification that "the invention is applicable to cache memory systems in general, and is not limited to the specific embodiment disclosed." '709 patent 4:22-26.

Freescale also erroneously argues that one of the objectives of the invention cannot be achieved when the cache is internal to the CPU. FSI Br. at 37-38. That assertion is wrong for multiple reasons, factual and legal. To begin with, Freescale has not explained why it believes the referenced statement ('709 patent, 73:48-49) articulates an "objective" of the invention. Even if it did, Freescale's argument misses the point of the discussion at column 73, lines 48-49. What that passage says is that the decoupling of buses accomplished by the claimed invention avoids the need for upgrading the system memory - that is true regardless of whether decoupling is accomplished by a cache that is internal or external to the CPU. Freescale's notion that an external cache makes the system more flexible is simply not tied to anything in the claims or the specification. Rather, the decoupling achieved by the design of the Chan patent's cache memory provides the flexibility to accommodate and support faster CPUs. Again, that is true whether the cache is on a separate chip or not, and thus the referenced passage does not suggest one way or another the use of an internal or external cache. In addition, FIG. 2, relied upon by Freescale in support of its argument, is a prior art illustration, where the cache does *not* accomplish decoupling of the processor from the system memory. It therefore bears no

relevance to the discussion in col. 73:48-49. Finally, even assuming for the sake of argument that Freescale were factually correct that an internal cache would not meet one of the several stated objectives set forth in the patent, that would not be dispositive. As the Federal Circuit made clear in Phillips, "[t]he fact that a patent asserts that an invention achieves several objectives does not require that each of the claims be construed as limited to structures that are capable of achieving all of the objectives." Phillips, 415 F.3d at 1327; citing Liebel-Flarsheim, 358 F.3d at 908.

Finally, Freescale asserts, without citing any legal support, that the claims of the Chan patents should be limited by depictions and drawings contained in preliminary product literature relating to a specific Mosel cache controller, the MS441, other portions of which Freescale believes may have been referenced in the Chan specification. FSI Br. at 39. This is a novel argument, one that runs afoul of the most basic tenets of claim construction. Merely because one particular Mosel product, which may or may not practice the patents-in-suit, also may have had an external cache does not mean that the claims of the Chan patents should be so limited. There simply is no basis for importing limitations into the express language of the claims from extrinsic, unrelated evidence such as product literature relating to the patentee's or third parties' products.

In contrast to Freescale's proposed construction of "cache memory," which is clearly aimed at avoiding a finding of infringement, ProMOS's proposed construction is directly supported by the claim language and the specification. See '709 and '241 patents, 2:60-65 (describing cache memory as a "small, fast, memory" maintained "locally" to the CPU to permit the "efficient use of low cost, high capacity DRAM memory"). It therefore should be adopted.

2. "host processor" and "host microprocessor," Chan 241, claims 1, 15:

ProMOS Construction	Freescale Construction
CPU associated with one or more cache memories	a single chip central processing unit (CPU)

Freescale asserts that "host processor" and/or "host microprocessor" both should be construed to mean "a single chip CPU." FSI Br. at 43-44. This construction improperly

confines the terms to a "single chip" – language that appears nowhere in the claim language, the specification, or the prosecution history. Freescale predicates its proposed construction on the assertion that "all examples in the specification are of single chip CPUs." FSI Br. at 44. However, as noted in Section I.A above, there is no basis for importing limitations from the examples in the specification into the plain and ordinary meaning of the claim terms. Freescale's proposed construction also reads the word "host" out of the claim terms by broadening the terms to refer to any processing unit, not just one that is associated with the cache memory. On this latter point, Freescale's assertion that "associated with" is "vague and confusing" misses the mark. FSI Br. at 43-44. As noted in both parties' discussion of the technology, the whole point of cache memory is that it "can be more quickly accessed" by the processor than system memory. FSI Br. at 17. The applicant's use of the word "host" connotes this functional association between the processor at issue and the cache memory. ProMOS's proposed construction of "host processor/host microprocessor" is designed to correlate with its proposed construction of "cache memory." Finally, Freescale is wrong in suggesting that "processor" and "microprocessor" have the exact same meaning, FSI Br. at 43, although the parties agree that both a processor and a microprocessor may be identified as a "CPU" in this context.

3. "system memory," Chan 241, claims 1, 15, 16:

<u>ProMOS Construction</u>	<u>Freescale Construction</u>
main memory of a computer, relatively larger and slower than cache memory	main memory of a computer system that is external to the CPU chip

Freescale's construction of "system memory" is defective for the same reasons as its construction of "cache memory": Freescale improperly seeks to limit the term to memory that is "external to the CPU chip," notwithstanding that this language appears nowhere in the patent, the specification, or the prosecution history. FSI Br. at 55. Freescale's only support for its proposed construction is the vague and unsubstantiated assertion that "[a]ll descriptions, figures, and embodiments in the specification show that the system memory is external to the processor." <u>Id.</u>

Freescale's attempt to import limitations from the embodiments into the claim language is improper and must fail. See argument in Section I.A, above.

4. "dual port cache memory," Chan 241, claims 1, 15, 16:

ProMOS Construction	Freescale Construction
A cache memory that has two interfaces	A cache memory chip having a host port and a system port

Freescale's construction of "dual port cache memory" suffers from the same defect as its construction of "cache memory" – both constructions seek to limit the term to a memory "chip" notwithstanding that this limitation appears nowhere in the claims, specification, or prosecution history. FSI Br. at 41-42. See Section I.A, above. Freescale also seeks to slip into this construction, by reference, its positions on "host port" and "system port." In contrast, ProMOS's construction comports with the ordinary meaning of the claim terms and should be adopted.

5. "host port," Chan '709, claims 1, 13, 17, 22; Chan 241, claims 1, 10, 16:

ProMOS Construction	Freescale Construction
Interface between a cache memory and a host processor or host data bus	A set of pins on the cache memory chip used for the input and output of data over the host data bus

Freescale concedes that a "port" is any "access point for data entry," but then attempts to limit that term's meaning to a "set of pins." FSI Br. at 40. The only support provided by Freescale for this position is the vague assertion (without citation to the specification) that the patents' embodiments "only" show pins. Id. Freescale's effort to import limitations from the embodiments into the claims must fail, for the reasons outlined in Section 1.A, above. In addition, Freescale's argument ignores that the specification and its embodiments repeatedly use the word "interface" to describe the host port. See, e.g., '709 patent, 73:3-6 (describing the host post 113 as "interfacing" with the CPU), 4:62-64 (FIG. 13 describes the host ports ("HP") as "the host interface between the 486 microprocessor and cache controller 70 and cache memory 72"). See also Ex. 7 to ProMOS Br. at 1642 (defining "port" as used in computer science as "an interface between a communications channel and a unit of computer hardware").

6. "system port," Chan 709, claims 1, 13, 17, 22; Chan 241, claims 1, 10, 16

ProMOS Construction	Freescale Construction
Interface between a cache memory and a system memory or system data bus	A set of pins on the cache memory chip used for the input and output of data over the system data bus

Freescale's proposed construction of "system port" fails for the same reasons as its proposed construction of "host port." FSI Br. at 40. In addition, as noted in ProMOS's Opening Brief, FIG. 14 in the patent shows the "system ports" (SP) of various portions of the cache memory 72 connected to the system bus, which in turn connects to system memory. The patent explains that FIG. 14 illustrates "the system interface between a system bus and cache memory 72 and cache controller 70" and thus the system port is an interface to the system memory and/or system bus. Again, Freescale is wrong in seeking to limit the term to a particular embodiment of "pins on the cache memory chip." ProMOS's construction thus should be adopted.

7. "register," Chan 241, claims 1, 10, 15, 16; Chan 709, claims 1, 2, 9, 13, 17, 22

ProMOS Construction	Freescale Construction
circuitry capable of retaining data or other information, such as address information	No definition proposed

Freescale has not formally proffered a proposed construction for "register," but it managed to come up with a definition when the need arose. FSI Br. at 53 (defining "register" as "a set of bits of high-speed memory within an electronic device used to hold data for a particular purpose.") Notably, however, the dictionary cited by Freescale purportedly in support of its proposed construction makes no mention of a "set of bits of high-speed memory used within an electronic device," and thus supports ProMOS's construction instead of Freescale's. FSI Br. at 53 n.44. ProMOS's proposed construction is consistent with the claims, the specification and the understanding of a person of ordinary skill in the art. See Ex. 8 to ProMOS Br. at 1103 (defining register as a "device capable of retaining information, often that contained in a small subset . . . of the aggregate information in a digital computer"). This construction makes clear the

meanings of 12 additional terms in the Chan patents that include "register," when those additional terms are read in context.[8]

8. "bus," Chan 241, claims 1, 15, 16:

ProMOS Construction	Freescale Construction
line or set of lines used to transfer data or other information	No definition proposed

Freescale addresses the term "bus" only in the context of offering proposed constructions for "host address bus" and "host data bus." FSI Br. at 44. For the reasons set forth in Section I.B.2.c, below, not only are Freescale's proposed constructions wrong because they improperly import limitations from the specification, but those terms also do not need to be construed by the Court if it provides a proper construction for the core term "bus." Although Freescale has not formally proposed a construction for the term "bus," its brief argues that the term means "a set of conductors used to transfer data between devices." FSI Br. at 44. None of the three dictionary definitions relied upon by Freescale in support of this definition require that the data be transferred "between devices," id. n.34, and nothing in the specification or prosecution history requires that the term be limited in such a manner. ProMOS's proposed construction is preferable because it comports with the understanding of one skilled in the art. See Ex. 8 to ProMOS's Opening Brief at 140-41; Ex. 7 to ProMOS's Opening Brief at 301.

9. "buffering," Chan 709, claims 1, 13, 17, 22; Chan 241, claim 1:

ProMOS Construction	Freescale Construction
storing data temporarily to compensate for differences in rates of data flow, time of occurrence of events, or amounts of data that can be handled by the devices or processes involved in the transfer or use of data	Using a storage element (e.g., memory write register) as an intermediary device to hold data temporarily while the data is waiting to be transferred from one external device (e.g., the CPU) to another external device (e.g., system memory) because of differences in rates of data flow or time of occurrence of events

Freescale's proposed construction of "buffering" includes a number of improper limitations designed specifically to support non-infringement positions. FSI Br. at 45-46. For

[8] Freescale initially proposed that "register" and each of its 12 variations should be construed separately by the Court. It later withdrew all but 7 of those "register" terms, which it now maintains are indefinite. As explained in Section I.B.2.e below, Freescale's indefiniteness positions are without merit.

example, Freescale seeks to limit the term "buffering" to the temporary storage of data transferred between separate devices that are "external" to one another, a limitation already discredited above. See Section I.A, above.[9] In seeking the inclusion of the "e.g." phrases referenced in its proposed construction, Freescale's construction also purports to apply its construction to exemplary circuitry of a memory system, thus seeking to fold infringement arguments into claim construction arguments. FSI Br. at 45. That effort is improper. Both of Freescale's arguments are based on the improper assertion that purported limitations from one of the embodiments should be read into the plain meaning of the terms, FSI Br. 45-46, and they should be rejected for the reasons set forth in Section I.A, *supra*. Buffering is a common term in the field of computing and has a well understood meaning among ordinary artisans, which meaning does not require an "external" device. Freescale effectively concedes as much in its brief by citing to dictionaries that do not support its proposed construction. FSI Br. at 47 n.35. ProMOS's proposed construction should be adopted because it is consistent with the meaning well understood by those in the art and consistent with the use of "buffering" in the claims.

10. "cache controller," Chan 241, claims 1, 16:

ProMOS Construction	Freescale Construction
Circuitry that controls the transfer of data or other information to and from cache memory	A chip that controls a cache memory chip

Freescale's proposed construction of "cache controller" provides no content other than to attempt, once again, improperly to limit the inventions of the Chan patents to cache memory located on a separate chip. FSI Br. at 42. As noted in Section I.A, Freescale's effort to import limitations from the specification and embodiments into the plain and ordinary meaning of the claim terms must fail. The remainder of Freescale's proposed construction merely states in a vague fashion that a controller "controls" a cache memory. Such a construction is akin to no construction at all. In contrast, ProMOS's proposed construction of "cache controller" comports

[9] Accord, e.g., Sun Studs, Inc. v. ATA Equipment Leasing, Inc., 872 F.2d 978, 989 (Fed. Cir. 1989) ("An apparatus claim describing a combination of components does not require that the function of each be performed by a separate structure in the apparatus"), overruled on other grounds by A.C. Aukerman Co. v. R.L. Chaides Constr. Co., 960 F.2d 1020 (Fed. Cir. 1992).

with the plain and ordinary meaning of the claim language and the specification, and therefore it should be adopted. See '241 patent, 4:3-14, 8:35-44, 8:60-65, 29:35-37.

11. Means-plus-function terms

11a. "means for *identifying* ones of the fetched data held in said memory update register as not corresponding to ones of the second data held in said write back register for write back to said system port," Chan 709, claim 10:

ProMOS	Freescale
Function: in italics above Corresponding Structure: the valid bits associated with the memory update register set 116	Indefinite – no corresponding structure disclosed in specification

Freescale argues that all of the means-plus-function claim terms contained in the Chan patents are indefinite because they lack corresponding structure. FSI Br. at 49-50. In doing so, Freescale apparently dismisses the corresponding structure identified by ProMOS (in the case of the "means for identifying ones of the fetched data," the valid bits associated with memory update register set 116, and in the case of the "means for masking," the mask bits associated with the memory update register 116) on the purported basis that "data values or bits … are not structure." FSI Br. at 50. In its Opening Brief, however, Freescale has provided no logical or legal support for the assertion that the valid bits and mask bits – which incorporate not only the data values but also the memory storage locations for such data values – are not sufficient structure. That failure is dispositive, as Freescale has the burden of proving indefiniteness by clear and convincing evidence. Aero Products Intern., Inc. v. Intex Recreation Corp., 466 F.3d 1000, 1015-16 (Fed. Cir. 2006).

In any event, it is well settled that the recited structure need not be hardware or even something that is solid to constitute sufficient structure, and that corresponding structure can include signals, instructions, software, and algorithms. See, e.g., Intel Corp. v. Via Tech., Inc., 319 F.3d 1357, 1365-67 (Fed. Cir. 2003) (signal may be corresponding structure); Altiris, Inc. v. Symantec Corp., 318 F.3d 1363, 1377 (Fed. Cir. 2003) ("batch files, commands, or instructions on a storage device" are corresponding structure); Overhead Door Corp. v. Chamberlain Group, Inc., 194 F.3d 1261, 1273 (Fed. Cir. 1999) (software is corresponding structure); Overhead Door

Corp. v. Chamberlain Group, Inc., 194 F.3d 1261, 1272 (Fed. Cir. 1999) (software operations are corresponding structure); WMS Gaming, Inc. v. Int'l Game Tech., 184 F. 3d 1339 (Fed. Cir. 1999) (algorithm is corresponding structure); Auction Management Solutions, Inc. v. Adesa Inc., Slip Op., 2007 WL 2698816, *17 (N.D. Ga. Sept. 11, 2007) (software is corresponding structure); STMicroelectronics, Inc. v. Motorola, Inc., 327 F. Supp. 2d 687, Appx. A (E.D. Tex. 2004) (specified signal was the corresponding structure). Freescale therefore has failed to meet its burden of demonstrating by clear and convincing evidence that the specification fails to provide sufficient corresponding structure for this means-plus-function term.

11b. "means for *identifying* *ones of the fetched data held in said memory update register as not corresponding to ones of the write back data held in said write back register for write back to said system port*," Chan 709, claim 26:

ProMOS	Freescale
Function: in italics above Corresponding Structure: the valid bits associated with the memory update register set 116	Indefinite – no corresponding structure disclosed in specification

The discussion in Section I.B.11.a above applies to this claim term. Freescale has waived any objection regarding this term by failing to present a logical or legal argument in its Opening Brief, although it bears the burden of production and persuasion on its indefiniteness defense.

11c. "means for *masking* *the providing of selected ones of said words of the fetched data to said random access memory*," Chan 709, claim 12:

ProMOS	Freescale
Function: in italics above Corresponding Structure: the mask bits associated with the memory update register set 116	Indefinite – no corresponding structure disclosed in specification

The discussion in Section I.B.11.a & b above applies to this claim term as well.

11d. "means for *masking* *writing of selected words of the system fetch data into said random access memory*," Chan 709, claims 21, 24:

ProMOS	Freescale
Function: in italics above Corresponding Structure: the mask bits associated with the memory update register set 116	Indefinite – no corresponding structure disclosed in the specification

The discussion in Section I.B.11.a & b above applies to this claim term as well.

11e. "<u>means for *masking*</u> *writing of selected words of data into said random access memory*," Chan 241, claims 26:

<u>ProMOS</u>	<u>Freescale</u>
<u>Function:</u> in italics above <u>Corresponding Structure</u>: the mask bits associated with the memory update register set 116	Indefinite – no corresponding structure disclosed in the specification

The discussion in Section I.B.11.a & b above applies to this claim term as well.

11f. "<u>means for *disabling*</u> *said dual port cache memory during a local bus access cycle*," Chan 241, claims 5, 19:

<u>ProMOS</u>	<u>Freescale</u>
<u>Function:</u> in italics above <u>Corresponding Structure</u>: Circuitry within the Controller 70 that evaluates host address and control signals and determines when a host bus cycle is not passed on to the system bus and does not cause a cache hit/miss determination. This includes the circuitry within Local Processor Interface Unit 220 and Control Register Interface Unit 224. Operation of the circuitry is described at 42:58-43:42, with reference to FIG. 37 and 38 and in Table VI at 39:27-35.	Indefinite – no corresponding structure disclosed in the specification

Freescale asserts that the "means for disabling" claim term is indefinite because the corresponding structure identified by ProMOS constitutes "undisclosed 'circuitry' inside the controller." FSI Br. at 50. Nothing could be further from the truth. ProMOS identifies the corresponding structure with a great amount of specificity; it identifies the circuitry's functions ("that evaluates host address and control signals and determines when a host bus cycle is not passed on to the system bus and does not cause a hit/miss determination") and it identifies specific structure included within the circuitry (see second sentence of proposed construction). It is well settled that this description is adequate in terms of identifying corresponding structure. <u>See</u> <u>S3, Inc. v. NVIDIA Corp.</u>, 259 F.3d 1364, 1370-71 (Fed. Cir. 2001) (a "selector" was adequate corresponding structure for performing the "selectively receiving" function even though neither the electronic structure of the selector nor details of its electronic operation were described in the specification); <u>Intel Corp. v. Via Tech., Inc.</u>, 319 F.3d 1357, 1365-67 (Fed. Cir.

2003) (generic core logic found to be adequate disclosure of structure even though no circuitry was disclosed in the patent to show how the core logic is modified). Freescale has fallen woefully short of meeting its burden of demonstrating through clear and convincing evidence in its Opening Brief that this claim term is indefinite.

C. Terms That Do Not Need to Be Construed, But That Freescale Nonetheless Has Proposed for Construction

For the reasons set forth in ProMOS's Opening Brief, the remaining terms proposed by Freescale for construction simply do not need to be construed, nor would it make any sense for the Court to attempt to construe them. See e.g., Lucent, 367 F. Supp. 2d at 657-66 (ruling that it was unnecessary for the Court to further construe claim terms the meanings of which could be understood without additional explanation from the Court, including "marking," "bytes," "node," "receiving a packet," "predetermined threshold," and "arrangement"). Nonetheless, should the Court decide to construe these terms, the constructions proposed by Freescale are not supported by the claim language, the specification, or the prosecution history.

1. "at the same time," Chan 709 claims 13 and 22

Freescale asks this Court to construe "at the same time" to mean "whenever" in the context of numerous claim phrases that include this term. FSI Br. at 49. The phrase "at the same time" has a plain and ordinary meaning and needs no construction by this Court. Paczonay v. Am. Recreation Prod., Inc., 2007 WL 295550 (N.D. Cal. 2007). If this Court were inclined to construe the term, however, Freescale's proposed "whenever" is not an adequate substitute for "at the same time." The latter connotes a temporal overlap while the former suggests a cause and effect relationship. It is hard to imagine any possible construction that would provide more clarity than the language used by the patentee, and therefore ProMOS respectfully suggests that this term needs no construction by the Court.

2. "first port" and "second port"; Chan 241 claims 1, 16

Freescale seeks construction of the terms "first port" and "second port." FSI Br. at 43. Neither of those terms needs to be construed, particularly if the Court adopts the construction of

"port" proposed above by ProMOS, because the claims of the patents themselves provide a description of what the terms means. The "first port" recited in claim 1 of the '241 patent has no independent meaning in the art, but rather is described in the claim itself as being a port connected to the host address bus. Similarly, the "second port" has no independent meaning in the art, but rather is described in the claims as being a port connected to the system address bus. Accordingly, construction of these terms is unnecessary, and any attempt to construe these claims would result in an impermissible exercise in redundancy. U.S. Surgical Corp. v. Ethicon, Inc., 103 F.3d 1554, 1568 (Fed. Cir. 1997).

To the extent the Court nonetheless decides to construe these terms, there is no basis for importing the "pin" and "chip" limitations into the plain language of the claims as proposed by Freescale, nor is there any basis for reading Freescale's suggested function for the ports ("used for the input and output of address information)" into the claim construction. FSI Br. at 43. As noted more fully in Section 1.B.1.e, *supra*, a "port" is understood in the art and used in the specification to refer to an "interface," not just a set of pins. ProMOS's alternative proposed constructions are more appropriate: "a port connected to the host address bus" (first port) and "a port connected to the system bus" (second port). These meanings are made clear from the claim language itself. '241 patent, 61:58-62, 64:11-14.

3. "host address bus" and "host data bus," Chan 241 claims 1, 15, 16

Freescale urges this Court to construe both "host address bus" and "host data bus." FSI Br. at 44. Neither of these terms needs to be construed because the meaning is clear from the claim language itself. That is particularly true because ProMOS has proposed that the Court separately construe the word "bus." Once that construction is completed, the meanings for these specific types of buses will be self-evident from the claims themselves, which specifically define what is meant by "host address bus" and "host data bus."

To the extent this Court nonetheless decides to construe the claim terms, Freescale's proposed constructions are untenable because they define each bus as a "set of conductors" connected to different "terminal pins" of a CPU "chip." Freescale's proposed constructions also

inappropriately include the phrase "used to transfer" and then seek to read into the terms a requirement that the bus actually be used in the manner specified. FSI Br. at 44. Freescale's proposed constructions clearly motivated by Freescale's anticipated non-infringement arguments and reflect an improper effort to import limitations from the specification into the plain language of the claims. ProMOS's construction is more simple, straightforward, and consistent with the claim language that already defines them. See Ex. 4 to ProMOS's Opening Brief at 7 (e.g., "host address bus" simply means a bus by which a host processor may provide an address).

4. "cache memory apparatus," "host," and "controller"

Freescale also proposes that three separate terms – "cache memory apparatus," "host" and "controller" – need to be construed, notwithstanding that the parties already have requested the Court to construe terms very similar to these terms. FSI Br. at 34-35, 43-44, 42. The term "cache memory apparatus" does not need to be construed once the term "cache memory" has been construed, because the meaning of "cache memory apparatus" will be clear without further effort by the Court. Moreover, the term "cache memory apparatus" need not be construed because it appears only in the preamble to the claims of the '709 patent, and the body of the claims themselves describe a structurally complete invention. See Intirtool, Ltd. v. Texar Corp., 369 F.3d 1289, 1295 (Fed. Cir. 2004) ("if the body of the claim 'describes a structurally complete invention such that deletion of the preamble does not affect the structure or steps of the claimed invention,' the preamble is generally not limiting unless there is 'clear reliance on the preamble during prosecution to distinguish the claimed invention from the prior art.'"). Similarly, the meaning of the term "controller" and "host" will be clear from the Court's construction of "cache controller," and "host processor," respectively.

5. various "register" terms that Freescale wrongly asserts are indefinite

In addition to the means-plus-function terms discussed in Section I.B.1 above and the incorrectly identified means-plus-function claims discussed in Section I.B.2.f below, Freescale also purports to contend that 10 additional terms are "indefinite." FSI Br. at 52-54. In order to sustain a finding of indefiniteness under § 112, ¶ 2, Freescale must prove by clear and

convincing evidence that the claim language at issue is not amenable to construction and is instead "insolubly ambiguous." Datamize, LLC v. Plumtree Software, Inc., 417 F.3d 1342, 1347 (Fed. Cir. 2005). If a term can be given "any reasonable meaning," it is not indefinite. Young v. Lumenis, Inc., 492 F.3d 1336, 1346 (Fed. Cir. 2007) (quoting Datamize, 417 F.3d at 1347).

But Freescale has not argued that the terms do not have any reasonable meaning to one skilled in the art or that they are "insolubly ambiguous." FSI Br. at 52-53. Rather, Freescale has argued that the terms, as they would be reasonably understood by one skilled in the art, are not adequately supported by the written description under § 112, ¶ 1. Id. at 53 ("ProMOS cannot claim concepts that it never conceived and never described in its original patent application."), 54 ("these terms do not satisfy the written description requirement"). But this argument is misplaced. Whether the patent satisfies the written description requirement of § 112, ¶ 1 is a question of fact that should be submitted to an evidentiary hearing, not decided in the Markman context. Cf. Intirtool, Ltd. v .Texar Corp., 369 F.3d 1289, 1294 (Fed. Cir. 2004) ("Compliance with the written description requirement is a question of fact, reviewed for clear error on appeal following a bench trial."). As noted in ProMOS's Opening Brief, the patent provides an ample description of the register terms. Even if it did not, however, that would not render the terms indefinite. Energizer Holdings, Inc. v. ITC, 435 F.3d 1366, 1369-70 (Fed. Cir. 2006).

Nor could Freescale have sustained an argument that the referenced "register" terms have no discernable meaning, had Freescale actually made an indefiniteness argument under § 112, ¶ 2. Seven of the claim terms Freescale contends are indefinite are terms that describe particular types of registers, e.g., "host input register," "system output register," and "first input register." See Ex. 4 to ProMOS Opening Brief at 9-11. The claim term "register" is discussed above in Section I.B, and Freescale has admitted in its brief that it has a definite meaning to one of skill in the art. FSI Br. at 53. Accordingly, Freescale is apparently contending that the adjectives such as "host input" used with register render these claim limitations indefinite. That position does not withstand scrutiny. In fact, Freescale's assertion that the referenced "register" terms are indefinite is belied by the fact that these terms were the subject of intense scrutiny by the

examiner during prosecution of the patents. FSI Br. at 25-28. After numerous rejections by the examiner on the issue of whether the "register" terms provided sufficient description and amendments by the patentee to address the examiner's concerns, even Freescale admits that the patentee "finally add[ed] enough structural and functional limitations describing how his invention worked and the Examiner allowed the claims." FSI Br. at 27. As discussed more fully in ProMOS's Opening Brief, the final, allowed claims contain register terms that describe their structure and function in a way that is unambiguous to one of ordinary skill in the art. The terms therefore are not indefinite.

6. "first sequencer for controlling" and "second sequencer for controlling"

Freescale also contends that the terms "first control sequencer for controlling" and "second control sequencer for controlling" are means-plus-function terms that are indefinite because no corresponding structure is disclosed in the specification. FSI Br. at 50-51. Freescale's argument fails because it is based on a faulty premise; these are not means-plus-function claim terms. It is well-established that "means-plus-function claiming applies only to purely functional limitations that do not provide the structure that performs the recited function." Phillips, 415 F.3d at 1311 (citing Watts v. XL Sys., Inc., 232 F.3d 877, 880-81 (Fed. Cir. 2000)). Freescale has conceded that if a claim element does not include the word "means," there is a presumption that the claim element is not in means plus function form governed by 35 U.S.C. § 112, ¶ 6. FSI Br. at 51. That presumption can be rebutted only by a clear demonstration that the claim element recites a function without sufficient structure for performing that function. Watts, 232 F.3d at 880. The Federal Circuit has cautioned, however, that the "presumption flowing from the absence of the term 'means' is a strong one that is not readily overcome." Lighting World, Inc. v. Birchwood Lighting, inc., 382 F.3d 1354, 1358 (Fed. Cir. 2004); see also DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc., 469 F.3d 1005, 1023-24 (Fed. Cir. 2006).

In the present case, Freescale has presented no evidence to support its assertion that the presumption should be overcome. FSI Br. at 51 (stating without support that "the presumption should be overcome because one skilled in the art would not know the precise structure for either

a first or second control sequencer"). Contrary to Freescale's conclusory assertion, one of ordinary skill in the art would readily understand that a control sequencer is a structure. See Ex. 7, *Mc-Graw-Hill Dictionary* at 1901 (defining sequencer as a machine which puts items of information into a particular order). Because these claim terms are not means-plus-function claim terms, there is no requirement that the specification identify corresponding structure and Freescale's indefiniteness argument falls of its own weight.[10]

7. "operably decoupled" and "decoupled from" (the latter appearing in a longer claim phrase), Chan 241, claim 1, Chan 709, claims 17 and 22

Freescale also contends that the term "operably decoupled" and a long phrase involving the term "decoupled from" are indefinite. FSI Br. at 51-52. Freescale's burden of proving indefiniteness is a heavy one. Energizer Holdings, Inc. v. ITC, 435 F.3d 1366, 1371 (Fed. Cir. 2006). Freescale's assertion that "operably decoupled" is indefinite boils down to an argument that "operably" would not be understood by one of ordinary skill in the art. FSI Br. at 52. But there is no basis for that contention. Claim 1 of the '241 patent uses the term "operably decoupled" in a manner that itself defines the term, reciting "wherein a data path between said host data bus and said system data bus is operably decoupled by buffering and selective provision of data to and from said cache storage locations by said plurality of registers so as to allow concurrent transfer of data to and from said dual port cache memory." Moreover, the term "operably" is commonly used in claim language and would be readily understood by a person of ordinary skill in the art. See Masco Corp. v. United States, 303 F.3d 1316, 1319-20 (Fed. Cir. 2002) (discussing patent claim term "operably"); DeMarini Sports, Inc. v. Worth, Inc., 239 F.3d 1314, 1319 (Fed. Cir. 2001) (same).

Freescale also argues that the term "decoupled from" is indefinite as used in the context of a longer claim phrase ("operations at said system port to be decoupled from said random

[10] Should the Court decide to construe these terms as ordinary terms and not means-plus-function terms, "first control sequencer" means "a first circuit which puts items of information into a particular order" and "second control sequencer" means "a second circuit which puts items of information into a particular order." See Ex. 4 to ProMOS's Opening Brief at 22.

access memory"). FSI Br. at 51. Freescale premises this argument on its own assertion that the operations at the system port cannot be decoupled from the RAM – an assertion that is factually incorrect and unsupported by the specification. See, e.g., '709 patent, 10:27-34 (memory write back register 118 buffers writes to the system port and memory update register 116 buffers reads from the system port), 33:1-11 (memory write back register 118 allows fetch to proceed without waiting for write back to system memory), 73:29-33 (same), 33:21-28 (memory update registers used to buffer data from system memory during fetches), 73:66-74:3 (processor and main memory accesses occur in parallel). It is worth noting that Freescale's argument is not relevant to the indefiniteness inquiry; rather it is an assertion of invalidity under § 112 ¶ 1, and a Markman hearing is not the appropriate place for resolving it. In any event, Freescale's assertion that it is unable to construe the phrase "decoupled from" is undermined by the initial claim charts it served in this case. In those charts, Freescale had no trouble understanding the term "decoupled from" and defined it in the following way: "allow different operations to occur concurrently without interference." Freescale's ability to understand this term undermines its position that the claim phrase "operations at said system port to be *decoupled from* said random access memory" is indefinite.[11]

8. "selectively providing," Chan 709 claims 1, 13, 17, 22

Freescale has asserted that the term "selectively providing" should be construed to mean "providing data held in a register depending on certain conditions and never providing the data held depending on other conditions." FSI Br. at 47. Unlike Freescale's proposed construction, the term "selectively providing" is not confusing. It is comprised of "commonly-understood English words [that] need no clarification." Netflix, Inc. v. Blockbuster, Inc., 477 F. Supp. 2d 1063, 1068 (N.D. Cal. 2007). Indeed, if the Court were to try to construe this term, there would be no way to define it more clearly than the claim language itself.

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11 If the Court were to construe the term "decoupled" or one of its variations, the patent supports the alternative construction offered by ProMOS in Exhibit 4 to its Opening Brief.

Nonetheless, if this Court is inclined to construe "selectively providing," Freescale's construction should not be adopted. Freescale's proposed use of the phrase "never providing data" is vague and unintelligible, certainly more so than the plain language used by the inventor. Moreover, it would be redundant and unnecessary to include any information regarding "data held in a register" in construing the claim term "selectively providing." ProMOS's alternative proposed construction is much clearer and makes more sense. See Ex. 4 to ProMOS's Opening Brief at 13 ("selectively providing" does not require construction, but if the Court were to provide a construction it means "providing or not providing depending on certain conditions.").

9. "selectively providing the first data to one of said random access memory, said system port, and said random access memory and said system port," Chan 709 claim 1

Freescale has also requested that the Court construe the long claim phrase "selectively providing the first data to ***one of*** said random access memory, said system port, and said random access memory and said system port" as requiring that the first data be provided to ***all three of*** the items rather than "***one of***" them. FSI Br. at 48. In essence, Freescale is seeking to rewrite the claim so that it says "all of" rather than "one of." Freescale's improper request that the Court re-write the claims in a manner that Freescale believes will suit its non-infringement positions must be rejected. SRAM Corp. v. AD-II Eng'g, Inc., 465 F.3d 1351, 1359 (Fed. Cir. 2006) ("we are powerless to rewrite the claims and must construe the language of the claims at issue based on the words used"). The same rationale applies to the other "selectively providing … to ***one of***" claim phrases identified by Freescale in its chart. FSI Br. at 48.

10. "buffering and selective provision of data to and from said cache storage locations by said plurality of registers," Chan 241 claim 1

Finally, Freescale has requested this Court to find the claim phrase "buffering and selective provision of data to and from said cache storage locations by said plurality of registers" indefinite because, Freescale asserts, "the patent specification … fails to disclose any register that is capable of performing the function of buffering and selective provision of data *from* said cache storage locations." FSI Br. at 54 (emphasis in original). Freescale is wrong to suggest that

the specification does not disclose registers capable of performing the recited functions. The specification describes such registers in detail. See, e.g., '709 patent, 10:27-34 (memory write back register 118 buffers writes to the system port and memory update register 116 buffers reads from the system port), 33:1-11 (memory write back register 118 allows fetch to proceed without waiting for write back to system memory), 73:29-33 (same), 33:21-45 (memory update registers used to buffer data from system memory during fetches), 73:66-74:3 (processor and main memory accesses occur in parallel). Even if it did not, however, that failure would not render the terms indefinite under § 112, ¶ 2, so long as the claim language itself could be construed. Energizer Holdings, Inc. v. ITC, 435 F.3d 1366, 1369-70 (Fed. Cir. 2006) (plain meaning of claim term "said zinc anode" referred back to the anode previously recited in the claim and therefore was not indefinite, notwithstanding ITC's determination that such construction made no sense in light of the specification). Finally, as with the "register" terms above, Freescale's written description arguments are not appropriately addressed in the Markman process.

II. PROPOSED CONSTRUCTIONS OF TERMS IN THE FORTIN '267 PATENT

A. Freescale's Opening Brief Reflects a Transparent and Improper Attempt to Inject Non-Infringement Arguments into the Claim Construction Process

Freescale's proposed constructions of terms in the Fortin patent are plainly crafted to accommodate anticipated non-infringement positions. Freescale begins its discussion of the Fortin patent by setting forth the basic semiconductor manufacturing steps used to form a tungsten plug and arguing that "[t]he Fortin patent claims certain alleged improvements in one way of carrying out these common steps – *a way that the accused processes do not use.*" FSI Br. at 3 (emphasis added); accord FSI Br. at 6 (asserting that "the accused HiP7 and HiP8 processes" use "CVD instead of PVD" and then urging the Court to construe the PVD claim term explicitly to exclude a process that involves any element of CVD). That approach to claim construction is improper as a matter of law. See, e.g., Intel Corp. v. Broadcom Corp., 172 F.Supp.2d 478, 487 (D. Del. 2001) (noting that it is improper to "consider the accused devices in construing the scope of the claims" and quoting Scripps Clinic & Research Found. v. Genentech, Inc., 927 F.2d

1565, 1580 (Fed.Cir.1991) ("claim terms should be construed independent of the accused product")). As this Court well knows, the Markman process properly focuses on a straightforward and honest reading of the claims in the context of the patents as a whole, without any attempt to compare the claims to an accused product or process or to grease the wheels for a ruling one way or the other on infringement.

B. Freescale's Proposed Constructions Of Terms In The Fortin Patent Are Not Supported By The Record And Embody Many Litigation-Driven Limitations

ProMOS objects on the following grounds to each of the constructions proposed by Freescale for the four terms from the Fortin patent that the parties identified for construction:

1. "rounding the top edge of the opening" (claims 1, 18, 25, 31, 42 and 47)

ProMOS Construction	Freescale Construction
Reducing the sharpness of the top edge of the opening	Indefinite

Freescale contends that the term "rounding" is indefinite, even though its brief evidences a clear understanding of what one skilled in the art would understand "rounding" to mean in this context. See FSI Br. at 8, 15-16 (complaining only that the patent does not specify how "rounding" accomplishes its stated objectives and that ProMOS's proposed construction has a "subjective" component). As ProMOS has explained, Freescale's burden on this score is a heavy one. See PRS Br. at 34. A claim will not be declared indefinite unless it is proven by *clear and convincing* evidence that the claim is so "insolubly ambiguous" that it cannot be understood by one of ordinary skill in the art. Metabolite Labs., Inc. v. Lab. Corp. of Am. Holdings, 370 F.3d 1354, 1366 (Fed. Cir. 2004); see Modine Mfg. Co. v. U.S. Int'l Trade Comm., 75 F.3d 1545, 1557 (Fed. Cir. 1996) abrogated on other grounds, Festo Corp. v. Shoketsu Kinzoku Kabushiki Co., Ltd., 234 F.3d 558 (Fed. Cir. 2000) (en banc) ("a patentee has the right to claim the invention in terms that would be understood by persons of skill in the field of invention"). Freescale has not met—and cannot meet—that heavy burden.

The specification describes in plain terms exactly what is meant by "rounding": "[T]he top surface of the structure [is] exposed to RF plasma in argon atmosphere for 10 seconds," which "smoothen[s] (round[s])" the top edges of the dielectric layer 110 to "reduce stress" and

"the risk of volcano formation." These "rounded" edges are specifically illustrated in Figures 4 and 5. Thus, one of ordinary skill in the art would readily understand that exposing the dielectric layer 110 "to RF plasma in argon atmosphere for 10 seconds" would produce exactly the sort of rounded edges illustrated in those Figures. Indeed, it is hard to imagine the inventor providing a clearer description – in both words and pictures – of what he meant by "rounding."

Freescale's indefiniteness argument rests on an assertion that the patent allegedly is not precise enough in teaching "the *degree* of rounding required to achieve the stated objective." FSI Br. at 16 (emphasis added). That argument is misplaced. It is well-settled that the sort of "[m]athematical precision" Freescale is seeking is not required in claim limitations. Modine, 75 F.3d at 1557; see also Seattle Box Co., Inc. v. Indus. Crating & Packing, 731 F.2d 818, 826 (Fed. Cir. 1984) (fact that "some claim language may not be precise . . . does not automatically render a claim invalid"). Because the specification and figures disclose sufficient information to enable one of ordinary skill in the art to understand what is meant by "rounding," this term is not indefinite.[12]

Freescale also contends that ProMOS's construction somehow "confirms" the limitation's indefinite nature, asserting that "sharpness," as used by ProMOS, is "subjective." FSI Br. at 16. That argument, however, ignores the relevant standard. The focus of the indefiniteness inquiry is on the claim language itself, not on a party's proposed construction of a term. A party's construction cannot render a claim indefinite. It is *the claim* that must be "insolubly ambiguous" in order to support a finding of indefiniteness. See, e.g., Exxon Research & Eng'g Co. v. United States, 265 F.3d 1371, 1380 (Fed. Cir 2001). In fact, the existence of a plausible claim construction is proof that the claim is not indefinite. See Bancorp Servs., LLC v. Hartford Life Ins. Co., 359 F.3d 1367, 1371 (Fed. Cir. 2004). In any event, Freescale is wrong in

[12] Freescale also suggests that "rounding" is indefinite because the patent discloses that preferred annealing parameters contribute to improved durability of the TiN barrier layer. See FSI Br. at 16 There is no logic to that argument. The fact that another feature may "contribute" to achieving the objectives identified in the patent does not make it impossible for one of ordinary skill in the art to practice the invention. Indeed, the patent claims both the rounding step and the annealing step (heating the TiN layer), and it precisely describes how each of those steps is carried out.

contending that the use of the word "sharpness" in ProMOS's proposed construction renders the "rounding" claim phrase indefinite. As the Federal Circuit recently made clear, the term "sharp" is sufficiently definite, and a claim construction need not specify precisely "how 'sharp' is too sharp." Acumed LLC v. Stryker Corp., 483 F.3d 800, 806 (Fed. Cir. 2007). For the reasons set forth above and in ProMOS's Opening Brief, the term "rounding the top edge of the opening" is not indefinite and it should be defined to mean "*reducing the sharpness of the top edge of the opening.*" [13]

2. "physical vapor deposition" (claims 1, 31, 47 and 52)

ProMOS Construction	Freescale Construction
A process [of accumulating material] in which films are deposited atomically by means of fluxes of individual neutral or ionic species [in a vapor phase] [14]	A process of building up material on a surface in which the material to be deposited is released from a source of the material into a vapor phase by one or more physical mechanisms. Chemical vapor deposition is not physical vapor deposition or a type of physical vapor deposition.

As explained in ProMOS's Opening Brief, its proposed definition of "physical vapor deposition" is taken directly from the Handbook of Semiconductor Manufacturing Technology ("Handbook") that is incorporated by reference in the patent. '267 patent, 4:49-56; Ex. 10 at 395. Freescale attempts to dismiss this significant intrinsic evidence by incorrectly alleging that ProMOS's definition of PVD uses "new, obscure terminology nowhere used by Fortin." FSI Br. at 12. Nothing could be further from the truth. ProMOS's definition comes straight from the Handbook that Fortin himself cited as embodying his understanding of PVD. [15]

[13] Unlike phrases such as "aesthetically pleasing" that may only be determined in the eye of the beholder, Datamize, LLC v. Plumtree Software, Inc., 417 F.3d 1342, 1350-51 (Fed. Cir. 2005), "sharpness" is a physical characteristic that is capable of objective analysis, particularly in view of the detailed description in the specification.

[14] In its Opening Brief, Freescale criticized ProMOS's definition of PVD for not defining "deposition" and not including any discussion of the "vapor" or gas phase. In order to address Freescale's objections, and to assist the Court in obtaining a resolution on contested constructions, ProMOS proposes the above revised construction that includes the additional text noted in brackets.

[15] Freescale's proposed construction is wrong for a number of reasons. Most importantly, it fails to give any credence to the Handbook, which is the main authority cited in the specification for the inventor's understanding of PVD, and which also identifies the distinguishing feature that differentiates PVD and CVD. See PRS Br. at 35 (discussing the concept of "flux" in the definition of PVD set forth in the Handbook incorporated by reference into the patent).

Because this intrinsic evidence makes clear what the inventor intended by PVD, there is no need to consult the extrinsic evidence cited by Freescale. Even if the extrinsic evidence cited by Freescale is considered, however, it is consistent with ProMOS's proposed construction. For example, the *Silicon VLSI Technology* paper cited by Freescale describes several "methods used to produce the *atom flux* in PVD." Ex. D to FSI Br. at 511 (emphasis added). Further, the excerpt cited by Freescale in Volume 1 of the textbook *Silicon Processing for the VLSI Era* contrasts PVD with a pure CVD process in which the important characteristic is to avoid so-called homogeneous reactions "because they form solid clusters ... [that] can *rain down* on the film growing on the wafers, which may cause defects in the depositing film." Ex. F to FSI Br. at 151 (emphasis added). In other words, this textbook teaches that CVD processes, in their pure forms, are characterized by the absence of flux (or raining down) of the depositing material, which supports ProMOS's position that flux, or lack thereof, is a defining characteristic as to whether a process includes PVD. [16]

Freescale also errs by spending a disproportionate amount of time discussing the alleged night-versus-day distinction between PVD and CVD. [17] As discussed above, that discussion is premature. To the extent Freescale believes that its HiP7 and HiP8 processes do not infringe the Fortin patent, because they use "CVD instead of PVD" to form the claimed TiN layer, that issue can and should be addressed through expert testimony at trial. Moreover, as ProMOS pointed

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[16] The processing technology textbook relied on by Freescale to support its construction of PVD (Freescale Ex. F) was known to the patentee. Specifically, to describe the tungsten CVD process referenced in the patent, Fortin incorporated by reference page 246 from Volume 2 of that textbook series. See '267 patent, 3:54-5. To the extent that any material difference exists between the description of PVD in the Handbook (which was specifically referenced in the patent) and the textbook submitted by Freescale (which was not), those differences reflect a deliberate choice by the patentee to incorporate by reference the publication that most accurately described the meaning he ascribed to PVD.

[17] ProMOS's proposed constructions also acknowledge the distinction between PVD and CVD. However, the approach adopted by ProMOS is different from Freescale in that (1) ProMOS includes in its definitions the distinguishing features of each process that are identified in the intrinsic record within the context of the invention, and (2) in ProMOS's proposed constructions, the essential differences between these processes are identified so that the distinction is evident in the definitions themselves, without the need for separate statements purportedly defining what each process is not. Freescale's contrary approach is not only unnecessary and wrong, it also runs the risk of confusing the jury.

out in its Opening Brief, Freescale's proposed definition of PVD relies on faulty circular reasoning that is inappropriate for purposes of claim construction and likely to confuse a jury. [18] Freescale's proposed "CVD is not PVD" construction is also wrong because it assumes that the world of thin film deposition is cleanly and completely divided between two, mutually exclusive types of processes. [19] Under Freescale's proposal, a given process could not meet the PVD limitation even if it contained both aspects of PVD and aspects of CVD. Such a construction cannot be correct. When the parties get to that stage of the case, the infringement analysis will focus on whether a given process meets all the limitations in a claim, and both PVD and CVD are limitations in different asserted claims of the Fortin patent. However, if an accused process satisfies a relevant PVD or CVD limitation, Freescale cannot avoid infringement simply because the process may include an additional, unclaimed element or step. See Free Motion Fitness, Inc. v. Cybex Int'l Inc., 423 F.3d 1343, 1347 (Fed. Cir. 2005) ("The addition of unclaimed elements does not typically defeat infringement when a patent uses an open transitional phrase such as 'comprising.' "); Dow Chem. Co. v. Sumitomo Chem. Co., 257 F.3d 1364, 1380 (Fed. Cir. 2001) ("It is fundamental that the use of [the] phrase ['which comprises'] as a transitional phrase does not exclude additional unrecited elements, or steps (in the case of a method claim).") (quotation omitted); Genentech, Inc. v. Chiron Corp., 112 F.3d 495, 501 (Fed. Cir. 1997) (same).

Finally, as discussed in Section II.B.4 below with respect to the claim term "sputtering," one result of Freescale's circular reasoning is that its proposed construction of PVD reads out the preferred embodiment in the patent in which the TiN layer is formed by reactive sputtering. Not only does reactive sputtering involve a chemical reaction (which Freescale apparently hopes to exclude from the definition of PVD by virtue of the language "CVD is not PVD"), but the nitrogen gas with which the titanium reacts is a vapor that is most certainly not formed by a

[18] By combining the arguments for PVD and CVD into a single section of its brief, Freescale seeks to obscure the logical fallacy of its position.

[19] The statements made by the inventor in the prosecution history were made in the context of the Fiordalice reference, which described and claimed a pure CVD process that did not include any elements of PVD. Moreover, the inventor's statements regarding that reference were intended to emphasize that the claims require a PVD process, not that they excluded any element of CVD. See FSI's Br. Ex. H at 9.

physical mechanism. Indeed, the fact that nitrogen is already a gas and does not need to be formed by a physical mechanism is evident from the fact that the air that we breathe comprises mostly nitrogen gas. Because Freescale's proposed construction of PVD is circular, incorrect, ignores the most relevant reference incorporated by reference in the patent, and reads out the preferred embodiment, it should be rejected. For the reasons set forth above and in ProMOS's Opening Brief, the term "physical vapor deposition" means "*a process of accumulating material in which films are deposited atomically by means of fluxes of individual neutral or ionic species in a vapor phase*."

3. "chemical vapor deposition" (claims 1, 23, 25, 31, 45, 47, 50 and 52)

ProMOS Construction	Freescale Construction
A process [of accumulating material] in which films are precipitated from the gas phase by a chemical reaction [of reactant species that have been transported to the deposition surface by thermal diffusion] [20]	A process of building up material on a surface in which a vapor formed with one or more chemical species that contain the material to be deposited, or components of the material to be deposited, undergoes suitable chemical reaction that enables the material being deposited to be released from the starting chemical species and accumulate on the deposition surface. Chemical vapor deposition is not physical vapor deposition or a type of physical vapor deposition.

Freescale's improper approach to claim construction is further illustrated by its treatment of the term "chemical vapor deposition." Reading its brief, one might conclude that this claim term is only directed to the forming of the claimed TiN layer, rather than the tungsten layer. Indeed, with the exception of a single remark buried in footnote 5, all of the discussion of the term CVD in Freescale's brief appears in connection with the discussion of forming the TiN layer by PVD. See FSI Br. at 6 (stating that "it is the use of PVD for the TiN layer that presents

[20] In its Opening Brief, Freescale criticized ProMOS's definition of CVD for not including or defining the concept of "deposition" in its proposed construction. In order to address Freescale's objection on that point, and to assist the Court in obtaining a resolution on contested constructions, ProMOS has revised its construction by proposing the additional text noted in the first set of brackets. To the extent that "precipitate" does not fully convey the diffusive motion of the vapor, the phrase in the second set of brackets has been added to capture more explicitly that concept.

the key issue for claim construction"). Thus, the focus of Freescale in discussing the claim term "CVD" is motivated by its erroneous position that any use of CVD to form the claimed TiN layer necessarily *excludes the use* of PVD (thereby side-stepping a PVD claim limitation), and its brief focuses on contrasting its accused processes with the PVD process disclosed in the claims, rather than on the meaning of CVD as used by the inventor in connection with forming the tungsten layer. Freescale's approach is backwards, confusing and wrong. ProMOS respectfully submits that the proper starting point for construing the claim term "CVD" should be where the term actually appears in the claims, rather than attempting to define it as the polar opposite of some other claim limitation altogether.

In its Opening Brief, ProMOS clearly explained the basis for its construction of the claim term CVD, as that term is used in the patent. See PRS Br. at 37 (explaining that ProMOS's proposed construction is taken directly from the pages of the Handbook that are incorporated by reference into the patent). It also bears noting, however, that ProMOS's position is further supported by the references attached to Freescale's brief. For example, the article attached as Ex. F to Freescale's brief teaches that in a CVD process, "the reactant-gas species are transported to the wafer surface ... by gas-phase diffusion." See Ex F at 150. Regardless of how the vapor is "released" from the source, the essence of CVD is this diffusive motion of the atoms and molecules. This discussion of CVD is entirely consistent with ProMOS's definition and, as discussed in ProMOS's Opening Brief, captures the critical, relevant feature of the claimed CVD process for depositing tungsten against which the TiN diffusion barrier was designed to protect.

There are a number of reasons why Freescale's circular definition of CVD cannot be accepted. Freescale contends that a CVD process not only needs to undergo chemical reaction, but also must *not* be released into the vapor phase by a physical mechanism. FSI Br. at 10. However, such a construction would again read out an embodiment disclosed in the specification. See '267 patent, 4:44-47 (explicitly stating that "the invention is applicable to different tungsten CVD techniques, including tungsten deposition from WCl_6 rather than WF_6."). As described by S. Wolf at page 246 of *Silicon Processing in the VLSI Era*, Vol. 2, which was

also incorporated by reference into the patent at 3:54-55, the tungsten CVD source material WF_6 is a liquid at room temperature, and WCl_6 is a solid at room temperature. See Ex. 11 at 245-46. These starting materials first need to be evaporated (evaporation being a recognized *physical* mechanism) into the vapor phase before it can be deposited onto a semiconductor wafer. Again, because it reads out a preferred embodiment, Freescale's proposed construction cannot be accepted. See Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576 (Fed. Cir. 1996).

Freescale's definition not only reads out the disclosed preferred embodiment, but is also inconsistent with the ordinary usage of the term in the art. Besides the two CVD embodiments in the patent, there are many other "CVD" techniques where the source material is stored as a liquid or a solid, therefore requiring a "release" into the vapor phase by a physical mechanism such as evaporation. See Ex. 12 (US Patent No. 6,007,330 to Gauthier which is directed to an apparatus devoted to such an application). As set forth in this and the preceding section, Freescale's claim construction positions are improper not only because they ignore the intrinsic reference and the embodiments disclosed in the patent, but also because they do not even accomplish Freescale's purported goal of distinguishing CVD from PVD and vice versa. For the reasons set forth above and in ProMOS's Opening Brief, the term "chemical vapor deposition" means "*a process of accumulating material in which films are precipitated from the gas phase by a chemical reaction of reactant species that have been transported to the deposition surface by thermal diffusion.*"

4. "sputtering" (claims 2, 25, 32, 48 and 54)

ProMOS Construction	Freescale Construction
A process in which atoms from near the surface of a material are physically dislodged by an incoming ion.	A type of physical vapor deposition in which a solid target is bombarded with high energy ions physically to dislodge the surface atoms on the target into a vapor phase for accumulation on the deposition surface without undergoing a chemical reaction.

Freescale contends that ProMOS's definition of this term "has no foundation in the art or the intrinsic record." FSI Br. at 15. That contention is meritless. ProMOS's proposed definition is taken directly from pages of a Handbook that are incorporated by reference in the patent. See

PRS Br. at 38 (citing '267 patent, 4:49-56; Ex. 10, Handbook at 396). Thus, ProMOS's proposed construction is taken from, and fully supported by, the intrinsic record; it is difficult to fathom how Freescale could say such a construction "has no foundation."

Moreover, even the extrinsic evidence cited by Freescale supports ProMOS's proposed construction. The Wolf textbook relied on in Freescale's Opening Brief states that "sputtering is a term used to describe the mechanism in which atoms are ejected from the surface of a material when that surface is struck by sufficiently energetic particles." Ex. F to FSI Br. at 438. That quotation is remarkably similar to ProMOS's position that "sputtering" means "a process in which atoms from near the surface of a material are physically dislodged by an incoming ion."

True to form, Freescale attempts to define "sputtering" *not* by explaining what it is, but rather by attempting to limit it exclusively to one type of thin film deposition technique ("a type of" PVD) and focusing on what it allegedly is not (i.e., a process that does not involve "a chemical reaction."). That approach is wrong for a number of reasons. First, the specification expressly states that "the invention is not limited to any particular sputtering process." '267 patent, 4:49-56. Nonetheless, Freescale's definition purports to limit "sputtering" to a type of PVD and to sputter *deposition* as opposed to sputtering processes that involve the *removal* of material. The inventor knew how to describe the concepts of "sputter deposited" ('267 patent, 3:6) and "deposited by reactive sputtering." '267 patent, 3:19-20. The claims do not use either of those terms, but instead use "sputtering" as a stand alone term without any modifying language related to the deposition of material.

The language of each of the claims in which "sputtering" appears requires that the TiN layer be "form[ed]" by "sputtering." The word "forming" does not necessarily equate to "depositing." Indeed, semiconductor devices are "formed" both by making deposits of layers and then selectively etching away portions of the deposited materials. Accordingly, "forming" is not limited to "depositing," and Freescale's unduly narrow proposed construction must be rejected for that reason as well.

Third, by asserting that sputtering is limited to processes in which accumulation occurs "without undergoing a chemical reaction," Freescale's proposed construction of "sputtering" would read out the preferred embodiment which discloses deposition by reactive sputtering. To form a thin film of the chemical compound titanium nitride with reactive sputtering, titanium atoms are sputtered off a solid piece of pure titanium (usually >99% purity) known as the target. The titanium then undergoes a chemical reaction with the nitrogen gas that is also present in the deposition chamber. If "a chemical reaction" disqualifies a process from qualifying as "sputtering," as Freescale suggests, the titanium nitride layer by definition cannot be formed in the manner described in the preferred embodiment disclosed in the Fortin patent. As noted in ProMOS's Opening Brief, a construction that reads out the preferred embodiment is "rarely, if ever, correct." Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576 (Fed. Cir. 1996).

Fourth, the following simple example shows the error in Freescale's proposed construction. As discussed in ProMOS's Opening Brief, the goal of the Fortin patent is to form thinner TiN films to solve the "volcano" problem. Claim 1 specifically requires a TiN film that is less than 25 nm. If a semiconductor manufacturer were to *deposit* a TiN layer by PVD that is greater than 25 nm, and then sputter away material until the layer is less than 25 nm, under Freescale's proposed construction the claim limitation would not be met. That would be true even though the final layer would be formed consistent with the limitations of the Fortin patent and would benefit from all of the recited advantages of the patented invention. Under Freescale's proposed construction, however, such a process would not practice the Fortin patent simply because its "forming the layer" step would involve both accumulation and removal of material. This illustration demonstrates that Freescale's unduly cramped proposed construction cannot possibly be correct. For the reasons set forth above and in ProMOS's Opening Brief, the term "sputtering" means "*a process in which atoms from near the surface of a material are physically dislodged by an incoming ion.*"

CONCLUSION

ProMOS respectfully submits that the Court should adopt ProMOS's proposed constructions of the disputed claim terms, as set forth in its Opening Brief and herein.

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EXHIBIT 11

SILICON PROCESSING FOR THE VLSI ERA

VOLUME 2: PROCESS INTEGRATION

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Third, the minimum size of the Metal 1 pad areas can be reduced, since any small grooves that might be etched alongside the pad during the via etch will be easily filled during the plug formation process (Fig. 4-39b). As a result, the pitches of both Metal 1 and Metal 2 can be reduced, allowing significantly increased packing density.

4.5.3 Processing Techniques that Allow for Vertical Vias

Two general fabrication approaches make the implementation of vertical vias possible:

1. *Filling of vias through deposition of metal into the opened via to form a plug in the opening.* In theory, this can be accomplished either independently of the metal-runner formation process, or through simultaneous fabrication of the plugs and metal runner. An example of the latter is the deposition and patterning of a blanket CVD W layer.

   On the other hand, when the plugs are formed separately, it is not necessary to replace the Al interconnect runners with those of a higher resistivity metal (W). Conversely, W contact plugs do not significantly increase the total resistance of interconnect lines because their length is so short (and because they maintain a large cross-sectional area): hence, they are appropriate for this use.

2. *Creation of a post, or pillar, which is then surrounded with a dielectric.*

Although the post approach offers several layout advantages, the plug approach is much easier to implement in a production-worthy process. Nevertheless, we will discuss both approaches.

4.5.3.1 Required Degree of Via Filling by Plugs. Although the plug structures described in the previous paragraphs will completely span the cross-sectional area of the contact holes or vias, they may not fill the openings up to the top. However, as noted earlier, adequate step coverage (e.g., >50%) by PVD metal into a vertically sided opening can still be achieved if the aspect ratio of the opening is less than 0.25. Step coverage by means of sputtered Al can thus be adequate under some circumstances, with more than 50% coverage possible in 1.2-μm wide, vertically sided, 600-nm-deep vias with 300-nm plugs. Figure 4-36b shows the step coverage of a 1.0 μm metal film into partially filled vias.[249]

4.5.4 CVD W Techniques for Filling Vertical Vias and Contact Holes

Two CVD W methods that have been developed for this application are *blanket CVD W and (etchback)* and *selective CVD W.*

4.5.4.1 General Information on the CVD Tungsten Process. The chemical vapor deposition (CVD) of tungsten is generally performed in either a hot-

wall, low-pressure system or a cold-wall, low-temperature system. Although tungsten can be selectively deposited either from WF_6 or WCl_6, the former (tungsten hexafluoride) is better suited as the W source gas, since it is a liquid that boils at room temperature (while WCl_6 is a solid that melts at 275°C). WF_6 can also be reduced by silicon, hydrogen, or silane, as shown by the following equations:

Silicon reduction

$$2WF_6 \text{ (vapor)} + 3Si \text{ (solid)} \rightarrow 2W \text{ (solid)} + 3SiF_4 \text{ (vapor)} \quad (4-12)$$

Hydrogen reduction

$$WF_6 \text{ (vapor)} + 3H_2 \text{ (vapor)} \rightarrow W \text{ (solid)} + 6HF \text{ (vapor)} \quad (4-13)$$

Silane reduction

$$2WF_6 \text{ (vapor)} + 3SiH_4 \text{ (vapor)} \rightarrow 2W \text{ (solid)} + 3SiF_4 \text{ (vapor)} + 6H_2 \text{ (vapor)} \quad (4-14)$$

When the hydrogen reduction is used, the rate-limiting step is the dissociation of H_2 into atomic hydrogen on the reaction surface. Selectivity is therefore achieved through deposition at a temperature below which SiO_2 will not catalyze the H_2 dissociation (~500°C), but at which other surfaces (silicon, metal, and silicide) will do so. If the entire surface is covered with a material that forms a good nucleating surface, the W will be deposited everywhere even when temperatures are below 500°C (*blanket W deposition*). If the nucleating surface exists only in certain locations (e.g., at the bottom of contact holes or vias), W will be selectively deposited in those locations. Above these temperatures, however, W will deposit on the SiO_2 as well. If the silane reduction is used, selectivity can be reproducibly achieved if the temperature is kept below 325°C, but it will be lost if the SiH_4/WF_6 flow-rate ratio is greater than 1.6.

On a silicon surface, the deposition starts with the silicon-reduction reaction (Eq. 4-12) even when hydrogen is present, and it will occur exclusively if hydrogen is absent. This reaction is self-limiting, however, since once a W layer is deposited it serves as a diffusion barrier between the Si and WF_6; the silicon reduction essentially stops when the W film reaches a thickness of 10-15 nm. For every two atoms of W deposited, three atoms of Si are consumed and volatilized as SiF_4. Typically, 10 to 15 nm of Si are consumed. No deposit occurs on the SiO_2 during the reaction. The silicon reduction of WF_6 can be used to produce thin films of selectively deposited W, with excellent surfaces and with sheet resistances of 10-15 Ω/sq.

The *hydrogen reduction process* can be used to selectively deposit thicker CVD W films, as was first reported by Blewer and Wells.[120] Normally, the silicon reduction reaction deposits the initial thin layer on a Si surface, and the hydrogen reduction then reaction takes over. As a result, the carrier gas at the outset the of this type of deposition is normally Ar. After the Si reduces the WF_6, either H_2 or SiH_4 is added to the gas flow, and the Ar flow is stopped.

EXHIBIT 12

US006007330A

United States Patent [19]

Gauthier

[11] Patent Number: 6,007,330

[45] Date of Patent: Dec. 28, 1999

[54] **LIQUID PRECURSOR DELIVERY SYSTEM**

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[73] Assignee: **Cosmos Factory, Inc.**, San Jose, Calif.

[21] Appl. No.: **09/041,843**

[22] Filed: **Mar. 12, 1998**

[51] **Int. Cl.**[6] **C23C 16/00**

[52] **U.S. Cl.** **432/47**; 427/248.1

[58] **Field of Search** 432/36, 47; 118/715, 118/725, 726, 720; 427/248.1, 255.1, 255.6

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,726,764	2/1988	Yoshikai	432/47
5,098,741	3/1992	Nolet et al.	427/248.1
5,451,260	9/1995	Versteeg et al.	427/248.1
5,492,724	2/1996	Klinedinst et al.	427/248.1
5,645,642	7/1997	Nishizato et al.	118/715
5,866,795	2/1999	Wang et al.	73/1.36

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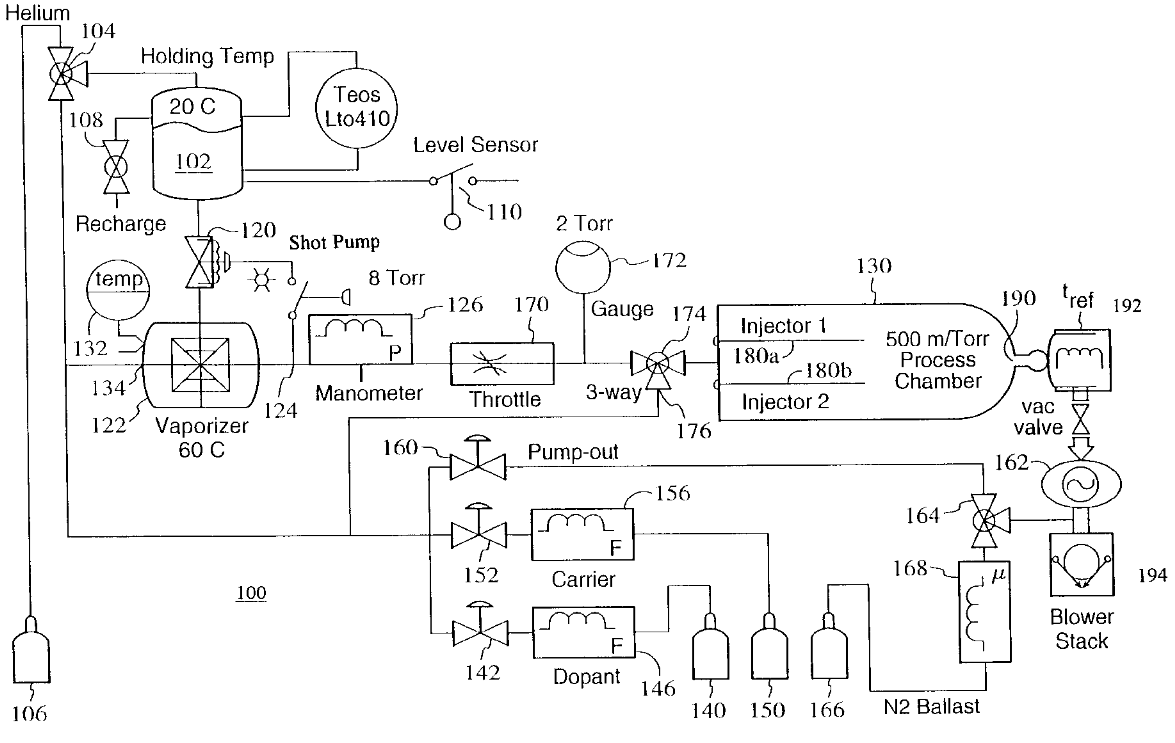
Assistant Examiner—Gregory A. Wilson
Attorney, Agent, or Firm—Ray K. Shahani, Esq.; David E. Newhouse, Esq.; Newhouse & Associates

[57] **ABSTRACT**

A system for delivering a liquid phase precursor fluid into a process chamber as a vapor phase fluid at constant pressure, the system comprising: a vaporizer for vaporizing the liquid phase precursor fluid prior to injecting the vapor phase fluid precursor into the process chamber, and a controllable device for transporting a preselected volume of the liquid phase fluid precursor from a reservoir to the vaporizer responsive to the pressure at the outlet of the vaporizer prior to entering the process chamber where the transport device is operated as the pressure at the outlet of the vaporizer canister drops, whereby system pressure perturbances are minimized prior to entering the process chamber.

4 Claims, 1 Drawing Sheet



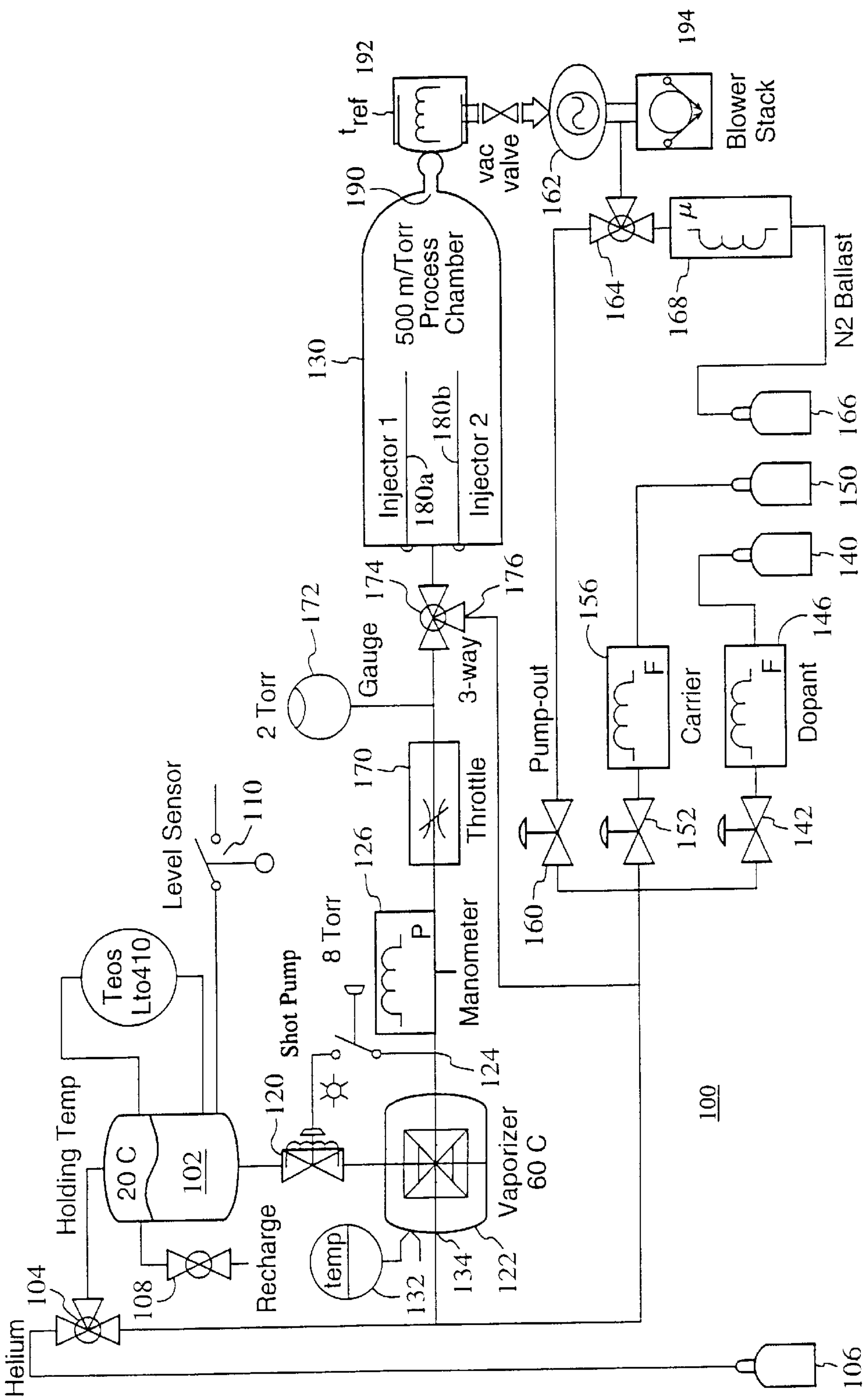

192
t_{ref}
190
vac valve
162
194
Blower Stack
500 m/Torr Process Chamber
130
164
168
N2 Ballast
Injector 1
180a
180b
Injector 2
166
150
140
174
176
172
Gauge
2 Torr
3-way
156
146
Pump-out
Carrier
F
Dopant
F
170
Throttle
Level Sensor
110
152
142
126
P
8 Torr
160
Manometer
Teos Lto410
Shot Pump
124
120
Holding Temp
20 C
102
Vaporizer 60 C
100
Recharge
temp
104
108
132
134
122
Helium
106

FIG. 1

LIQUID PRECURSOR DELIVERY SYSTEM

FIELD OF THE INVENTION

The present invention relates to delivery of liquid phase precursor fluids for chemical vapor deposition (CVD) and similar mass transport processing operations typically used in the manufacture of semiconductor wafers.

More particularly, the invention relates to a method and apparatus for implementing dual proportional-integral-derivative (P.I.D) type servo control over output pressure and operating temperature, hence flow of a vapor phase precursor, by controlling input of a liquid precursor component and thermal energy to a vaporizer.

BACKGROUND OF THE INVENTION

Chemical vapor deposition (CVD) processes are typically utilized in production of integrated electronic semiconductor components in which numerous layers of various types of materials are deposited one layer at a time onto a Silicon or other semiconductor substrate wafer. In a typical CVD manufacturing process, round wafers of extremely pure silicon, germanium or other semiconductor substrate typically of a diameter between 2 and 12 inches, comprise a base onto which layers of conducting, semi-conducting and insulating materials are successively deposited. Gates and paths as well as circuit elements are etched into each successive layer, usually by photolithic and laser illumination processes. In this way the layers are interconnected forming an integrated array of electronic processing devices and circuits. Several dozen to several hundred identical individual integrated circuits/devises are typically simultaneously deposited onto a single wafer at a time. The deposited base wafer is then cut up to into individual devices or "chips" either before or after they are electronically tested for defects. The individual chips are then incorporated into electronic devices, such as computer boards, toys, household electronics, automobile circuits, manufacturing equipment, commercial equipment, and the like.

The CVD process is typically described in terms of temperature-dependent phase change and nucleation/deposit phenomenon and typically involves reactions and commingling of one or two vapor phase fluids or gases in combination with a reactive surface. In many instances the source of the reactant gas is fluid in liquid phase which must be vaporized with minimum perturbation of vapor phase fluid pressure, temperature and volume parameters in the process or reaction vessel to achieve uniform, well formed layers of deposited materials. In other words, as in other precision manufacturing processes, limits and tolerances are narrow.

In the prior art, numerous designs for reaction chambers and parameters are described for achieving the rigorous operating conditions in chemical vapor deposition processes for depositing integrated semiconductor circuits. For example, U.S. Pat. No. 5,091,219 to Monkowski et al issued Feb. 25, 1992 describes a CVD process which requires specific geometries and flow patterns of the reactant gases within an essentially cylindrical reactor. This patent teaches that uniformity and control over layer deposition is accomplished by directing flow pattern of reactant gas through the reactor.

U.S. Pat. No. 5,098,741 to Nolet et al issued Mar. 24, 1992 teaches a method and system for delivering liquid reagents to processing vessels wherein a volume of liquid reagent is metered to an expansion valve with an adjustable orifice which increases and decrease in diameter responsive to up stream of the liquid pressure. The liquid reagent flashes

to vapor phase as it passes through to the downstream side of the expansion valve which typically is at a much lower pressure. Energy (heat) is supplied to the downstream side of the expansion valve, i.e., a vaporization chamber or vaporizer located upstream from the reactor vessel to provide necessary heat of vaporization to prevent fogging and droplet formation. The point of the adjustable orifice in the expansion valve is to minimize perturbations in the pressure of vapor phase reagent (mass flow rate) downstream of expansion valve due to inert gases dissolved in the liquid reagent upstream from the expansion valve.

U.S. Pat. No. 5,320,680 to Learn et al issued Jun. 14, 1994 teaches a primary flow CVD apparatus comprising gas preheater and a geometry promoting substantially eddy-free gas flow. This patent attempts to describe an operative reaction chamber with a hot wall reaction tube, and primary and secondary reaction gas preheaters vessels each with gas injectors directing heated gas into an annular mixing zone immediately upstream of the cylindrical reaction tube. The idea is that the reactant gases are preheated as they are injected into the annular mixing zone which because of its coaxial relationship with the reaction tube promotes highly laminar reactant gas flow through the tube perpendicular to the edges of wafers stacked in boats within the reaction tube. Preheating immediately upstream of the reaction tube and laminar flow perpendicular to stacked wafer edges is thought to reduce wafer contamination due to premature nucleation (particle formation) of the reactant gases, eddies and stagnant regions within the reaction tube volume. Learn et al doesn't discuss problems associated with a liquid phase source for the primary or secondary reactant gases.

U.S. Pat. Nos. 5,361,800, 5,371,628 and 5,437,542 issued Nov. 8, Dec. 6, 1994 and Aug.1, 1995, respectively, to Ewing describe direct liquid injection positive displacement liquid pump and vaporizer systems. The automated valve pumping systems use a pair of pumps operating in opposition to provide continuous and constant volumetric flow of liquid to a vaporizer using a stack of disks heated for flashing the liquid reagent to vapor the liquid.

U.S. Pat. No. 5,421,895 to Tsubouchi issued Jun. 6, 1995 et al teaches an apparatus for generating and then vaporizing small droplets of liquid phase reactant comprising a piezoelectric vibrator vibrating an open nozzle tip for ejecting a liquid droplets at ambient pressure into small pores through a heated plate into a vapor chamber maintained at substantially lower pressure.

U.S. Pat. No. 5,510,146 to Miyasaka issued Apr. 23, 1996 teaches a CVD apparatus and method of fabricating a thin-film semiconductor device. This low-pressure system produces a thin film forming a channel portion inside a reaction chamber in which the pressure is reduced at a specified rate at the commencement of the procedure.

U.S. Pat. No. 5,620,524 to Fan et al issued Apr. 15, 1997 teaches a system based upon a continuous delivery, micro metering pump pumping a liquid phase reagent fluid to provide a continuous flow pulse-free vapor phase reagent flow manner depends on the capacity and restrictive connection of the pump to its external environment, as well as the electronic control circuitry and control algorithms used to control the motion of the displacement elements of the pump.

However, an alternative approach to achieving a uniform, controllable and effective layer deposition on a substrate is to utilize a liquid precursor system with feedback control based on the pressure and temperature of the vaporized precursor relative to an initial stage vaporizer. The prior art

does not teach the use of a controller for a liquid shot pump which receives an operating signal from a pressure transducer measuring the pressure of a temperature controlled front end vaporizer.

SUMMARY OF THE INVENTION

The present invention is a method and apparatus for forming a semiconductor layer by chemical vapor deposition of any liquid phase precursor material by vaporization of the liquid phase, and (optional) premixing with either or both carrier and dopant gases prior to injection into a process chamber where the wafers are deposited. The system uses a first temperature controlled liquid canister for containing the liquid phase precursor fluid and a second temperature controlled vapor canister for vaporizing the liquid phase precursor material. A liquid shot pump controlled by a signal produced in response to the pressure of the system measured by a manometer communicates liquid phase precursor material from the first liquid phase canister to the vapor phase canister as the pressure, which is constantly monitored, starts to drop due to the mixture of vapor phase precursor material and/or carrier gas and/or dopant gas being drawn off into the process tube or reactor. The vapor phase canister is temperature controlled at an optimum vaporization temperature level for the precursor.

Also connected to the vaporizer canister is a source of carrier and/or dopant gas and associated valves, for prehomogenization of the gases before entering the reaction or process chamber. Mass flow controllers (MFCs) control flow of the various gases, including nitrogen or other purge system, for fast clearing of the entire gas system if necessary. Residual effluent gases are drawn off at the opposite end of the process tube and collected in a condensate trap to protect a vacuum system from contamination. Loading or filter burden is monitored through the use of pressure transducers or other sensors differentially compared and read by the main controller.

Thus, it is an advantage of the present invention to provide an apparatus and method for forming a uniform, electronically uniform, stable and other with applicable and advantageous characteristic, layer or film of semiconductor material by chemical vapor deposition.

It is another advantage of the present invention to provide an apparatus and method for forming such layer of semiconductor material by chemical vapor deposition in a low pressure reactor.

It is another advantage of the present invention to provide an apparatus and method for forming such layer of semiconductor material in which a liquid precursor material vaporizer canister is charged by a liquid precursor at a rate based on fluctuation in pressure at the outlet of the vaporizer, as implemented using a PID or other servo control scheme.

It is another advantage of the present invention to provide an apparatus and method for forming such layer of semiconductor material in which the liquid precursor material vaporizer canister is maintained constant at an optimum temperature.

Numerous other advantages and features of the present invention will become readily apparent from the following detailed description of the invention and the embodiments thereof, from the claims and from the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a representative system diagram for forming a semiconductor film or layer by the apparatus and method of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

It will be understood that while numerous preferred embodiments of the present invention are presented herein, many of the individual elements and functional aspects of the embodiments are similar. Therefore, it will be understood that structural elements of the numerous apparatus disclosed herein having similar or identical function will have like reference numerals associated therewith.

FIG. **1** is a representative system **100** diagram for forming a semiconductor film or layer by the apparatus and method of the present invention. Liquid canister **102** is temperature controlled. An optimum temperature for holding liquid precursors is determined based on their relatively high cost and relatively low life at elevated temperatures, and can be selected randomly or based on other parameters as well. In a preferred embodiment, the temperature of the liquid precursor stored in canister **102** will be maintained between about 5 degrees Celsius and about 100 degrees Celsius, and more preferably at about 20 degrees Celsius or other temperature, and at any appropriate pressure, for preserving the precursor under conditions in which its shelf life is longest. Typically, reagent grade precursors are used, i.e. precursors having an ultra-high purity and suitable for the manufacture of semiconductor devices. Especially with regard to some liquid precursors, since their decay time is shorter at elevated temperatures, it is desirable to hold the typical liquid precursor materials at as low a temperature as possible relative to the temperature at which it is vaporized in the process chamber **130**.

The nature of the liquid precursor material will depend on the type of process which is being performed in the process chamber **130**. For CVD, diffusion and other processes, typical liquid precursor materials together with the corresponding solid phase material which is deposited on or diffused into a wafer are set forth in Table 1 as follows.

TABLE 1

Liquid Reagent	Material Deposited
Trichlorosilane	Epitaxial Silicon
Dichlorosilane	Epitaxial silicon
Tetraethylorthosilicate (TEOS)	SiO_2, phosphosilicate glass
Trimethylborate (TMB)	Borophosphosilicate glass
Trichloroethane	Oxide passivation
Boron tribrornide	Boron diffusion
Phosphorous oxychloride	Phosphorous diffusion
Fluorotriethoxysilane (FTES)	SiOF films
Tetrakis-dimethylamino Titanium (TDMAT)	Titanium nitride films
Tetrakis-diethylamino Titanium (TDEAT)	Titanium nitride films
CuTMVS	Copper films
Trimethylcyclotetrasiloxane (TOMCATS)	SiO_2 films
Diethylsilane	SiO_2 films
Triethylborate (TEB)	Borosilicate glass and borophosphosilicate glass
Trimethyl Phosphite (TMPI)	Liquid phosphorous for SiO_2 doping
Triethylphosphate (TEPO)	Liquid phosphorous for SiO_2 doping

A three way valve **104** is connected to liquid canister **102**. In one position, helium from helium storage container **106** flows into storage container **102** for maintaining positive pressure therein. In a preferred embodiment, helium from storage tank **106** pressurizes liquid canister **102** through the normally open channel of the three way valve **104**. Upon depletion of an initial charge of liquid precursor, liquid canister **102** can be recharged by closing the open channel

through three way valve **104** from helium tank **106** to liquid canister **102** and opening the closed channel. This negatively pressurizes the liquid canister **102**. By attaching a recharge vessel (not shown) to recharge valve **108** and opening said valve, a volume of liquid precursor will flow through recharge valve **108** into liquid canister **102**. Thereafter, once the canister **102** has been recharged, the recharge valve **108** can be closed and the three way valve **104** switched to repressurize the canister **102** with helium or other carrier or purge gas. Thus, utilizing a level sensor **110** or other means for determining remaining volume of liquid precursor in liquid canister **102**, the canister can be automatically or manually refilled and the system **100** operated essentially continuously.

Shot pump **120** communicates liquid precursor to vaporizer canister **122**. The shot pump **120** is controlled in a feedback loop control system in which the pressure of the output **124** of vaporizer **122** is measured using manometer **126**. As the vaporized liquid precursors, carrier gases and/or dopant gases are drawn out of the vaporizer **122** into process chamber **130**, the resultant drop in pressure will trigger the shot pump **120**. Preferred embodiments of the shot pump of the present invention have an orifice diameter about 0.001 inches and about 0.5 inches, and more preferably about 0.040 inches. Such shot pumps are also known as “bio-solenoids”, and are similar to those used in processes such as gas and/or high pressure liquid chromatography. Typically, such shot pumps **120** or bio-solenoid valves will have a Teflon or other resilient, polymeric insert for providing a high repetition pulse rate.

In a preferred embodiment, the vaporizer **122** is maintained between about 500 Torr and about 0.5 Torr, and more preferably at about 8 Torr. Vaporizer canister **122** will be temperature controlled by controller **132** and maintained at the optimum vaporization temperature for the precursor, such as between about 5 degrees Celsius and about 100 degrees Celsius, and more preferable at about 60 degrees Celsius or other temperature. This temperature in conjunction with the reduced pressure of the vaporizer **122** will result in rapid vaporization of the liquid precursor or precursors introduced into the canister. Another port **134** allows the introduction of a carrier gas, dopant, or other fluid into the vaporizer **122**. This introduction of carrier gases, dopants or other fluids into the vaporizer **122** rather than directly into the process chamber **130** pre-homogenizes the gases, along with the vaporized liquid precursor or precursors, so as to develop a uniform and evenly dispersed gas mixture within vaporizer **122**.

Additional gas and/or fluid transport systems are part of the present system **100**. In a preferred embodiment, the liquid precursor system uses a dopant gas which is maintained in dopant reservoir **140** and a carrier gas or fluid maintained in carrier reservoir **150**. Dopant is delivered through valve **142** as controlled by mass flow controller **146**. Carrier gas or fluid is delivered to the system through valve **152** as controlled by mass flow controller **156**. An additional valve **160** can be used for pumping out the system with vacuum source **162** through three way valve **164**, and also for purging the system **100** such as with nitrogen gas from nitrogen storage tank **166** through mass flow controller **168**. Dopants include boron, phosphine and other compounds, such as those used for P-N doping, etc.

Between the process chamber **130** and the manometer **126** at the outlet **124** of the vaporizer **122** there is a restriction or other pressure reducing valve (PRV) **170**. Gauge **172** provides a means for determining the pressure within the system at that stage, i.e. prior to another three-way valve **174**. Flow through valve **174** is therefore either by liquid precursor downstream of PRV **170** or by other gas or fluid from input **176**. Flow out of valve **174** is directed into one or two or more injectors, such as **180***a* and **180***b*, etc., within a process chamber **130**. Pressure within the process chamber **130** will, in preferred embodiments, be reduced, such as to between about 50 mTorr and about 500 Torr, and more preferably about 500 mTorr. The temperature of the process chamber will, in preferred embodiments, be elevated to between about 25 degrees Celsius and about 500 degrees Celsius, and more preferably to about 250 degrees Celsius.

It will be understood that any of various different embodiment of the reaction or process chamber **130** will be known to those skilled in the art. In particular, specific configurations and systems are known for automated or assisted handling of wafer stacks in and out of the process chamber, and will be included within the scope of the present invention. In particular applications, wafers are stacked onto “boats” or support trays through which the gases injected into the process chamber **130** can circulate in the preferred flow character.

Residual effluent gases are drawn out of the process chamber **130** at a distal end **190**, and through condensate trap **192**. This trap **192** protects the vacuum system from contamination. Across both the inlet and the outlet of the trap **192** are pressure transducers. Differential comparison of the signals from such transducers are determined and read by a main controller. When a specific setpoint or other predetermined level of loading across the trap **192** is determined, the system controller can send an alarm to instruct an operator to change or otherwise regenerate the trap **192**. The vacuum source **162** with its associated blower stack **194** provides a way to pump out any andlor all of the various channels.

Integral to the present invention is the control scheme or algorithm used to servo the shot pump controller based upon the pressure at the outlet of the vaporizer. In preferred embodiments, a PID controller with a vaporizer outlet pressure setpoint is used. In a preferred embodiment, a dual PID controller with individual set points and corresponding gains for temperature and pressure both can be used. Variable gain controllers are used in preferred embodiments of the present invention.

The system of the present invention is unique also in the pressure buffering which is possible. Liquid precursor is injected into a vaporizer at a rate so as to maintain an outlet pressure of at least about 8 Torr. The pressure of the gas is throttled down to about 2 Torr, at which point it is injected into the reaction or process chamber **130** which is maintained at or about 500 mTorr. The nitrogen dump and/or ballast can be used to control pressure throughout the system **100**. This unique pressure buffering scheme is advantageous for providing non-variable, uniform, homogeneous and well defined semiconductor layers, as desired. The pressure control scheme enhances pumpdown, purge, cleaning and evacuation procedures to pressures as low as 50 mTorr.

Unless defined otherwise, all technical and scientific terms used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this invention belongs. Although any methods and materials similar or equivalent to those described can be used in the practice or testing of the present invention, the preferred methods and materials are now described. All publications and patent documents referenced in this application are incorporated herein by reference.

While the principles of the invention have been made clear in illustrative embodiments, there will be immediately

obvious to those skilled in the art many modifications of structure, arrangement, proportions, the elements, materials, and components used in the practice of the invention, and otherwise, which are particularly adapted to specific environments and operative requirements without departing from those principles. The appended claims are intended to cover and embrace any and all such modifications, with the limits only of the true purview, spirit and scope of the invention.

I claim:

1. A method for delivering a liquid precursor material from the liquid state at or near atmospheric pressure to a reduced pressure in which the precursor material exists as a vapor, the method comprising the following steps:

providing a system comprising means for containing the liquid precursor material, means for vaporizing the liquid precursor material, and means for transporting the liquid precursor material to the means for vaporizing in which liquid precursor which is transported into the vaporizer canister is vaporized and drawn off through an outlet into a process chamber;

determining the pressure of the system at a point adjacent the outlet of the vaporizer canister; and

maintaining the pressure of the system as determined at the point adjacent the outlet of the vaporizer canister at a setpoint by dispensing a predetermined amount of liquid precursor into the vaporizer when the determined pressure is below the setpoint.

2. The method of claim **1** in which the system further comprises a pressure transducer and a controller which, during the step of maintaining the pressure adjacent the outlet of the vaporizer canister of the system at the setpoint, causes the means of transport of liquid precursor material to transport a predetermined amount of the liquid precursor material into the vaporizer when the determined pressure is below the setpoint.

3. The method of claim **1** in which the means for containing the liquid precursor material is temperature controlled, the method further comprising the step of maintaining the temperature of the liquid precursor material at a selected temperature.

4. The method of claim **1** in which the means for vaporizing the liquid precursor material is temperature controlled, the method further comprising the step of maintaining the temperature within the means for vaporizing the liquid precursor material at a selected temperature.

* * * * *